

# IGMLSB V:1.0

## AIO330 Gemini Lake

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9	SOC SD/EMMC/LPC/FSPI/HDA	33	+1V8_S5/+1V05_S5S0/+VPP
10	SOC PMU/RTC/SVID	34	+1V24_S5/+1V2_MEM/+0V6_MEM
11	SOC Power/VCC/VNN	35	ISL95854HRZ/+VCGI_SVID
12	SOC Power/VDDQ/VCCIO/Other	36	ISL95854HRZ/+VNN_SVID
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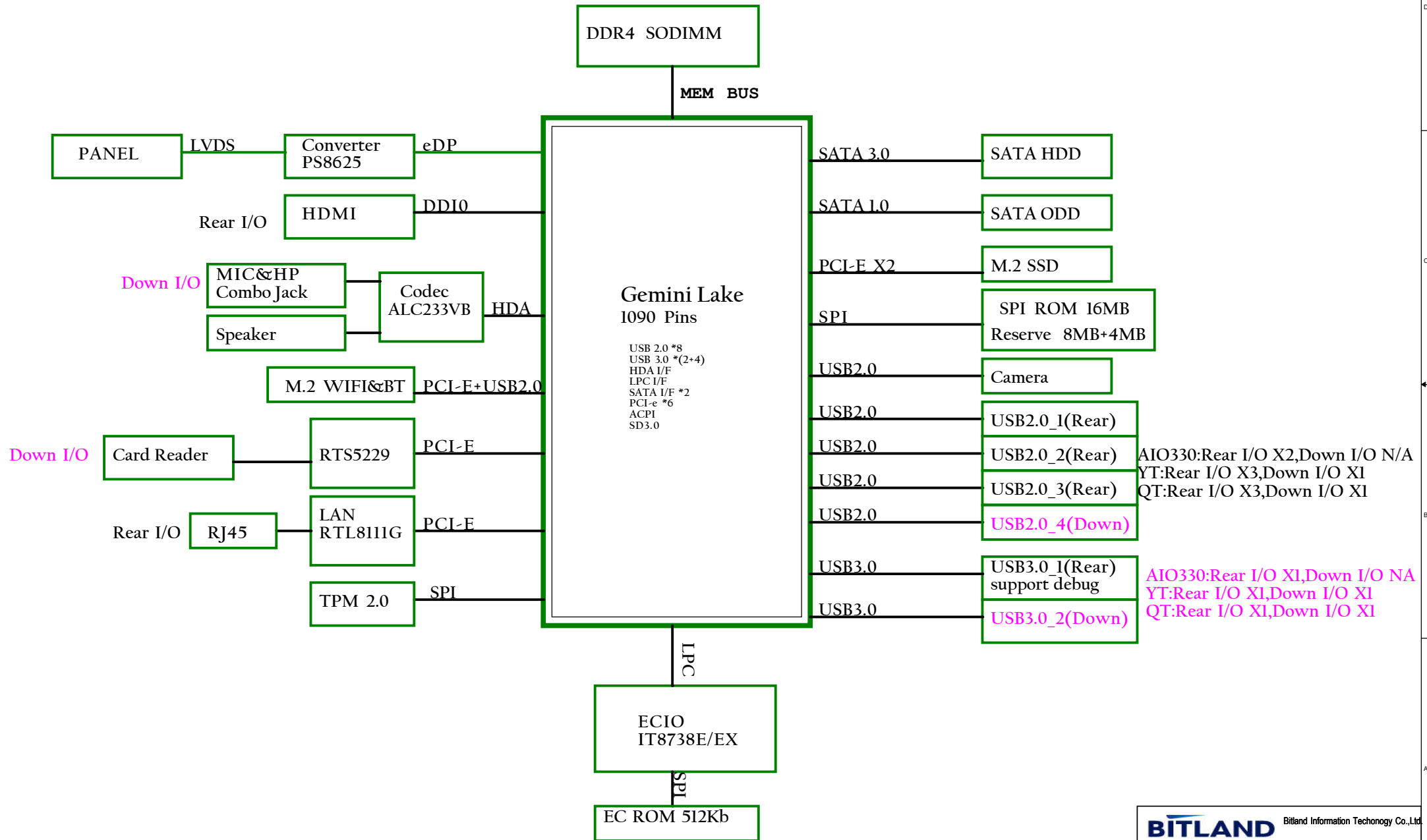
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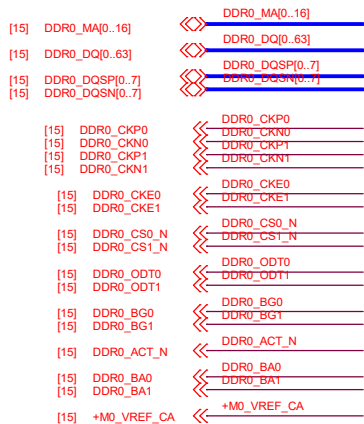
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EDS: 569262\_GLK\_EDS\_Vol1\_Rev1p2.pdf

CHECKLIST: 569092\_GLK\_SchmChklst\_Rev1p2.docx

# System Block Diagram





Byte 5

Byte 4

Byte 7

Byte 6

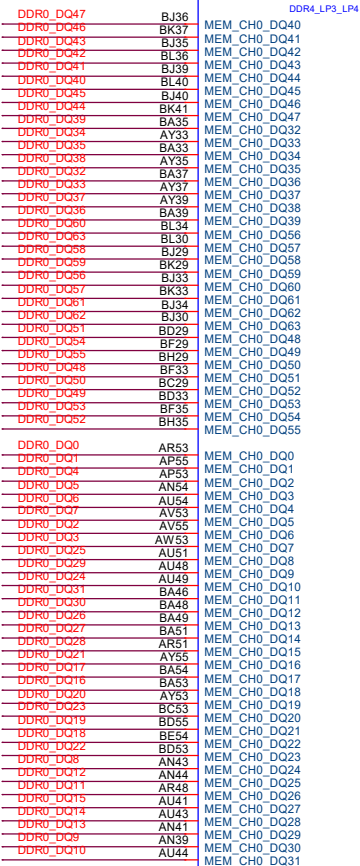
Byte 0

Byte 3

Byte 2

Byte 1

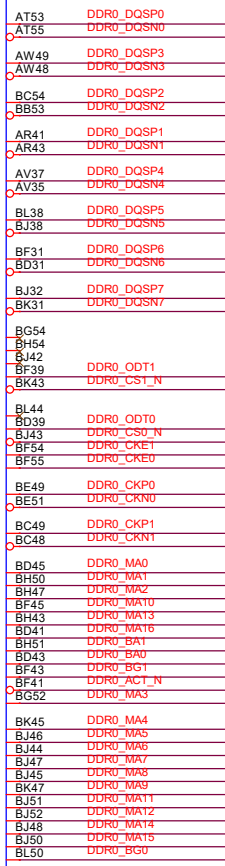
0405 Daniel  
Swap Byte 1 with Byte 3



CPU1A

DDR4\_LP3\_LP4

DDR4\_LP3\_LP4



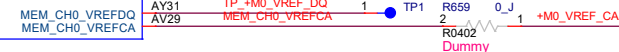
Byte 3

Byte 1

0405 Daniel  
Swap Byte 1 with Byte 3

GLK\_SOC\_RVP1

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CPU1B

DDR4\_LP3\_LP4

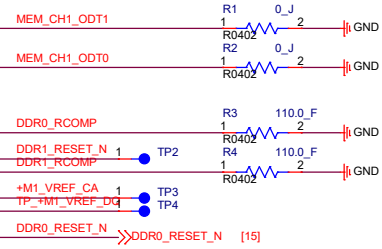
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AY3 MEM\_CH1\_DQ40  
BD3 MEM\_CH1\_DQ41  
BC3 MEM\_CH1\_DQ42  
AY1 MEM\_CH1\_DQ43  
BA3 MEM\_CH1\_DQ44  
BE2 MEM\_CH1\_DQ45  
BE2 MEM\_CH1\_DQ46  
AR8 MEM\_CH1\_DQ47  
AN18 MEM\_CH1\_DQ32  
AN17 MEM\_CH1\_DQ33  
AU12 MEM\_CH1\_DQ34  
AN12 MEM\_CH1\_DQ35  
AN13 MEM\_CH1\_DQ36  
AU13 MEM\_CH1\_DQ37  
AU18 MEM\_CH1\_DQ38  
AP3 MEM\_CH1\_DQ39  
AU2 MEM\_CH1\_DQ56  
AV3 MEM\_CH1\_DQ57  
AW3 MEM\_CH1\_DQ58  
AN2 MEM\_CH1\_DQ59  
AP1 MEM\_CH1\_DQ60  
AR3 MEM\_CH1\_DQ61  
AV1 MEM\_CH1\_DQ62  
AR5 MEM\_CH1\_DQ63  
BA8 MEM\_CH1\_DQ48  
AU7 MEM\_CH1\_DQ49  
AU5 MEM\_CH1\_DQ50  
BA5 MEM\_CH1\_DQ51  
BA5 MEM\_CH1\_DQ52  
AU9 MEM\_CH1\_DQ53  
BA10 MEM\_CH1\_DQ54  
X MEM\_CH1\_DQ55  
BJ26 MEM\_CH1\_DQ0  
BL26 MEM\_CH1\_DQ1  
BJ27 MEM\_CH1\_DQ2  
BK27 MEM\_CH1\_DQ2  
BJ23 MEM\_CH1\_DQ3  
BK23 MEM\_CH1\_DQ4  
BJ22 MEM\_CH1\_DQ5  
BJ22 MEM\_CH1\_DQ6  
BD22 MEM\_CH1\_DQ7  
BF27 MEM\_CH1\_DQ8  
BH27 MEM\_CH1\_DQ9  
BC27 MEM\_CH1\_DQ10  
BH21 MEM\_CH1\_DQ11  
BF23 MEM\_CH1\_DQ12  
BD23 MEM\_CH1\_DQ13  
BF21 MEM\_CH1\_DQ14  
BK19 MEM\_CH1\_DQ15  
BJ20 MEM\_CH1\_DQ16  
BL20 MEM\_CH1\_DQ17  
BJ21 MEM\_CH1\_DQ18  
BJ17 MEM\_CH1\_DQ19  
BJ18 MEM\_CH1\_DQ20  
BK15 MEM\_CH1\_DQ21  
BL18 MEM\_CH1\_DQ22  
BA21 MEM\_CH1\_DQ23  
AY25 MEM\_CH1\_DQ24  
BA23 MEM\_CH1\_DQ25  
BA17 MEM\_CH1\_DQ26  
AY21 MEM\_CH1\_DQ27  
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AY19 MEM\_CH1\_DQ29  
AY19 MEM\_CH1\_DQ30  
BA19 MEM\_CH1\_DQ31

DDR1

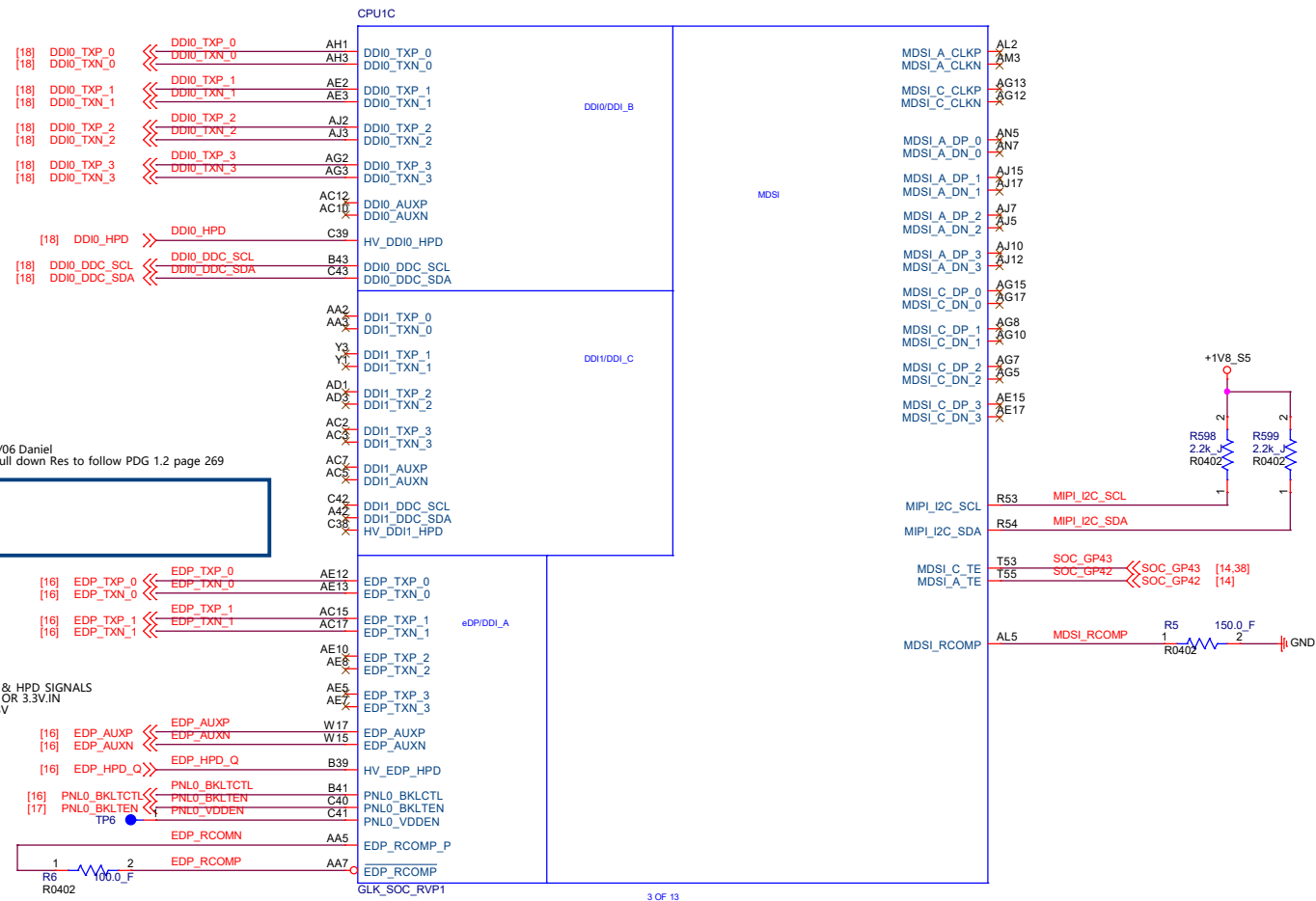
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MEM\_CH1\_DQS1  
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MEM\_CH1\_DQS2  
MEM\_CH1\_DQS3\_P  
MEM\_CH1\_DQS3  
MEM\_CH1\_DQS4\_P  
MEM\_CH1\_DQS4  
MEM\_CH1\_DQS5\_P  
MEM\_CH1\_DQS5  
MEM\_CH1\_DQS6\_P  
MEM\_CH1\_DQS6  
MEM\_CH1\_DQS7\_P  
MEM\_CH1\_DQS7  
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MEM\_CH1\_MA1  
MEM\_CH1\_MA2  
MEM\_CH1\_MA3  
MEM\_CH1\_MA10  
MEM\_CH1\_MA13  
MEM\_CH1\_MA16  
MEM\_CH1\_BA0  
MEM\_CH1\_BA1  
MEM\_CH1\_BG1  
MEM\_CH1\_ACT  
MEM\_CH1\_MA11  
MEM\_CH1\_MA12  
MEM\_CH1\_MA14  
MEM\_CH1\_MA15  
MEM\_CH1\_BG0  
MEM\_CH1\_MA4  
MEM\_CH1\_MA5  
MEM\_CH1\_MA6  
MEM\_CH1\_MA7  
MEM\_CH1\_MA8  
MEM\_CH1\_MA9  
MEM\_CH1\_CLK0\_P  
MEM\_CH1\_CLK0  
MEM\_CH1\_CLK1\_P  
MEM\_CH1\_CLK1  
NCTF3  
NCTF4  
NCTF1  
NCTF2  
MEM\_CH1\_CS1  
MEM\_CH1\_ODT1  
MEM\_CH1\_CS0  
MEM\_CH1\_ODT0  
MEM\_CH1\_CKE0  
MEM\_CH1\_CKE1  
MEM\_CH0\_RCOMP  
MEM\_CH1\_RESET  
MEM\_CH1\_RCOMP  
MEM\_CH1\_VREFCA  
MEM\_CH1\_VREFDQ  
MEM\_CH0\_RESET

BJ24  
BK25  
BD25  
BF25  
BL18  
BL18  
AV19  
AV21  
AR13  
AR15  
BB3  
BC2  
AW7  
AW8  
AT1  
AT3  
BH9  
BC13  
BD11  
BD13  
BF11  
BE5  
BH5  
BH6  
BF13  
BG4  
BE7  
BK11  
BJ12  
BK9  
BJ11  
BJ10  
BJ4  
BL6  
BJ5  
BJ9  
BJ6  
BJ8  
BF17  
BD17  
BF15  
BH15  
BJ13  
BL12  
BF1  
BF2  
BC7  
BH2  
BC8  
BG2  
BK13  
BJ14  
AY29  
BC15  
AY27  
AY27  
AY27  
AY25  
AY25  
BC43



GLK\_SOC\_RVP1

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32	1'h0	<b>PANEL0_BKLTCTL</b> <b>(vccio_pad_panel0_bkltctl):</b> 0 = PAD VCCIO is 3.3V ( <b>default</b> ) 1 = PAD VCCIO is 1.8V
----	------	--

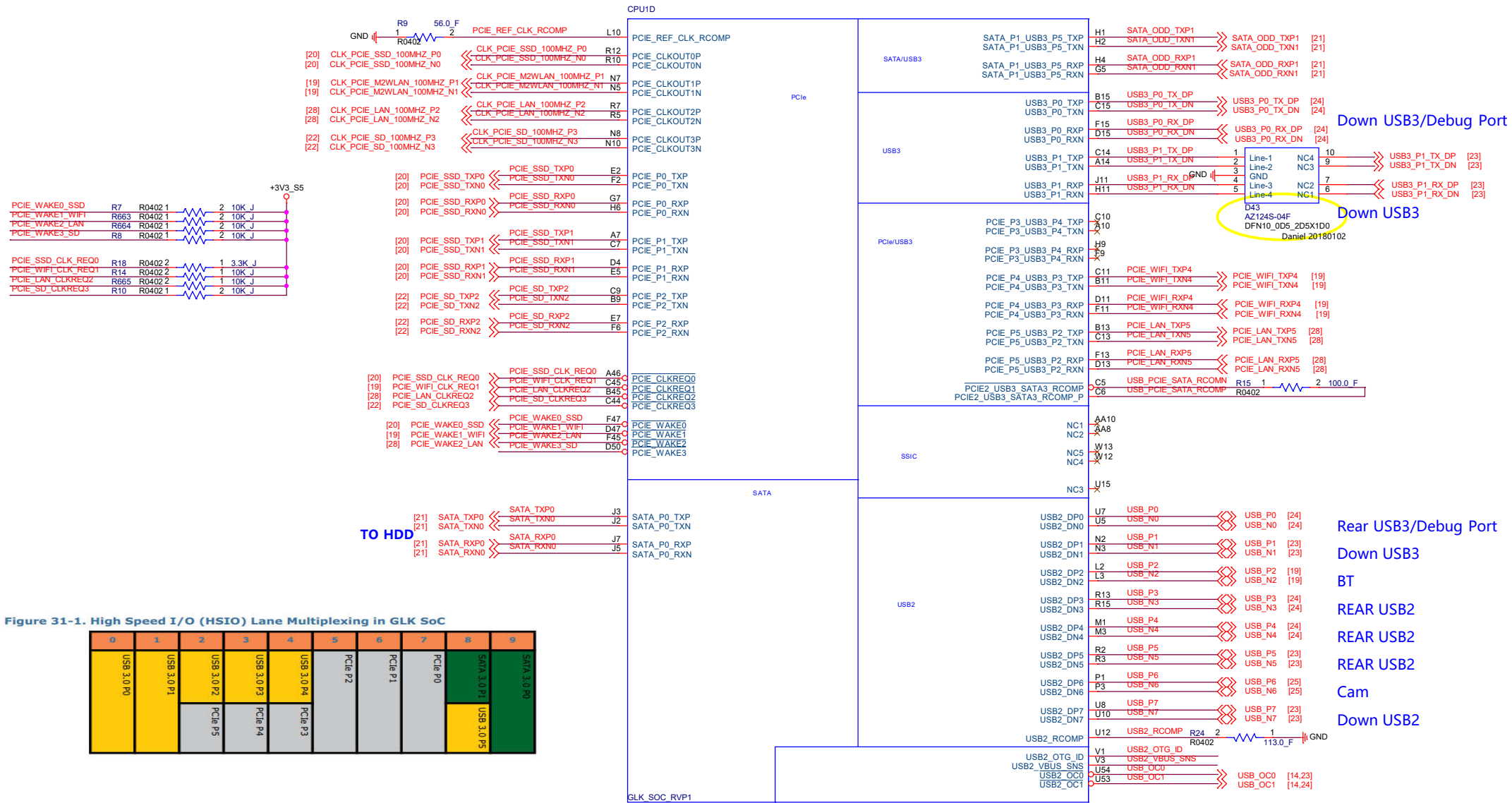


Figure 31-1. High Speed I/O (HSIO) Lane Multiplexing in GLK SoC

### 3.9.1 PCIe\* Port Mapping

Table 3-28. PCIe\* Port Mapping

PCIe* Config.	Pin #	Function	Root Port/BSR	Signal Names	Bifurcation
x2	20	0/Direction (RP0)	0/Direction (RP0)	PCIe_P0_USB3_P1_Tx/Rx	1 x2, 2 x1
	21	1/Direction (RP0)	1/Direction (RP0)	PCIe_P0_USB3_P2_Tx/Rx	
x4	20	0/Direction (RP0)	0/Direction (RP0)	PCIe_P0_USB3_P1_Tx/Rx	1 x4, 2 x2, 2 x1, 4 x1
	21	1/Direction (RP0)	1/Direction (RP0)	PCIe_P0_USB3_P2_Tx/Rx	

Note: For proper functionality of the PCIe\* ports, each CLKREQ signal must be associated with the corresponding CLKREQ2 signal to enable the clocks. Ensure that the BIOS assigns a valid number for the CLKREQ.

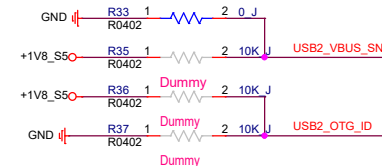
Table 3-29. Supported Configurations for x4 Root Port

Configuration	Port 0	Port 1	Port 2	Port 3
1 x4				
2 x2	x3	x4	x2	
1 x2, 2 x1	x3	x1	x1	x1
4 x1	x3	x1	x1	x1
2 x1, 1 x3	x1	x1	x2	

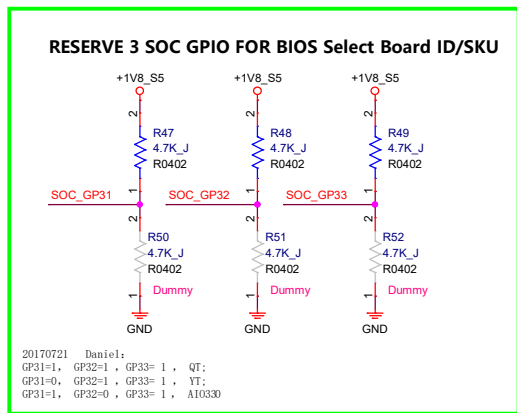
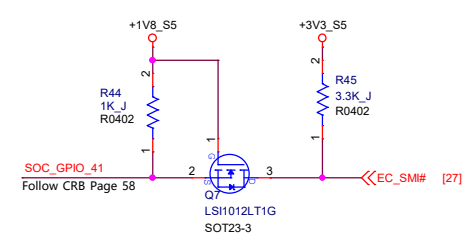
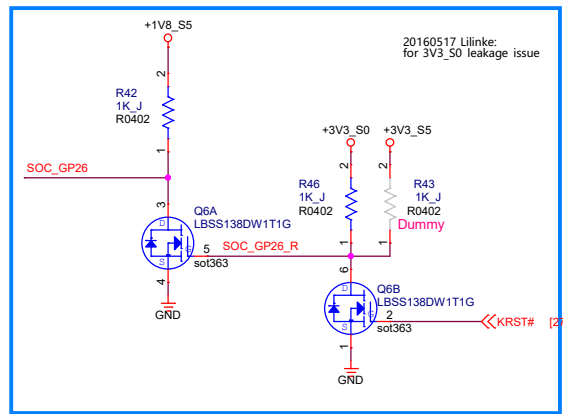
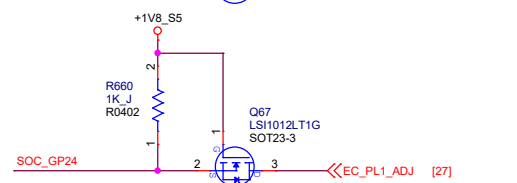
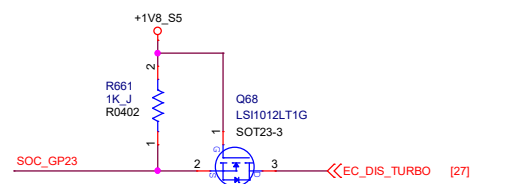
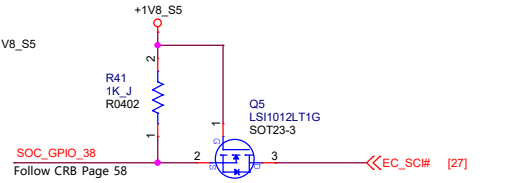
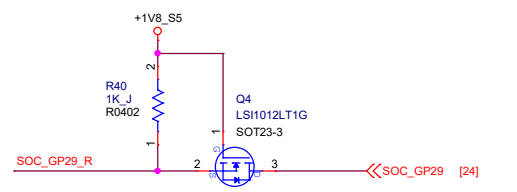
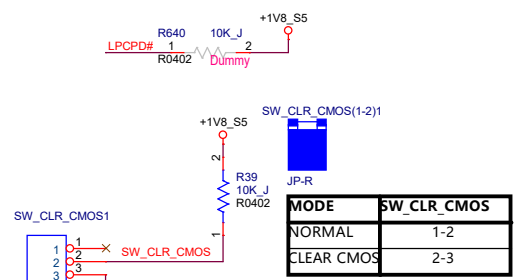
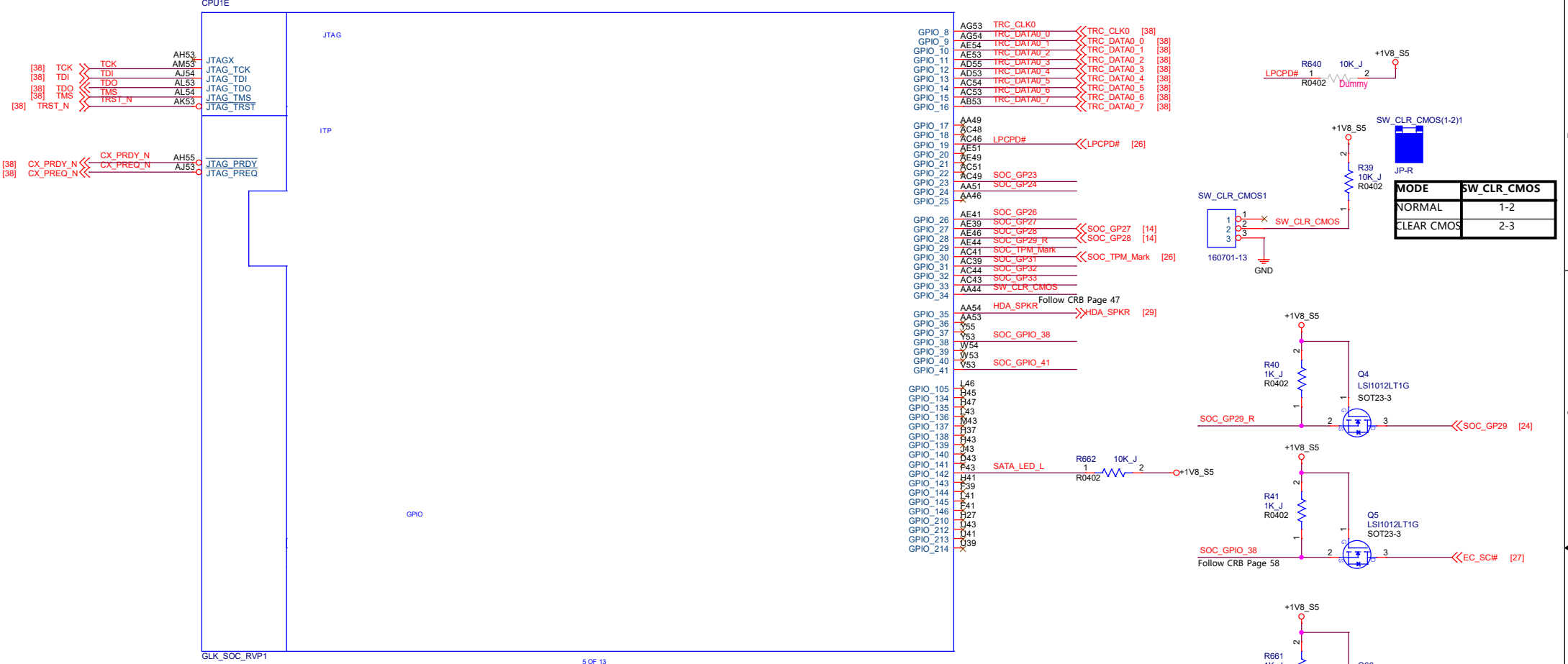
Table 3-30. Supported Configuration for x3 Root Port

Configuration	Port 0	Port 1
1 x3	x2	
2 x1	x1	x1

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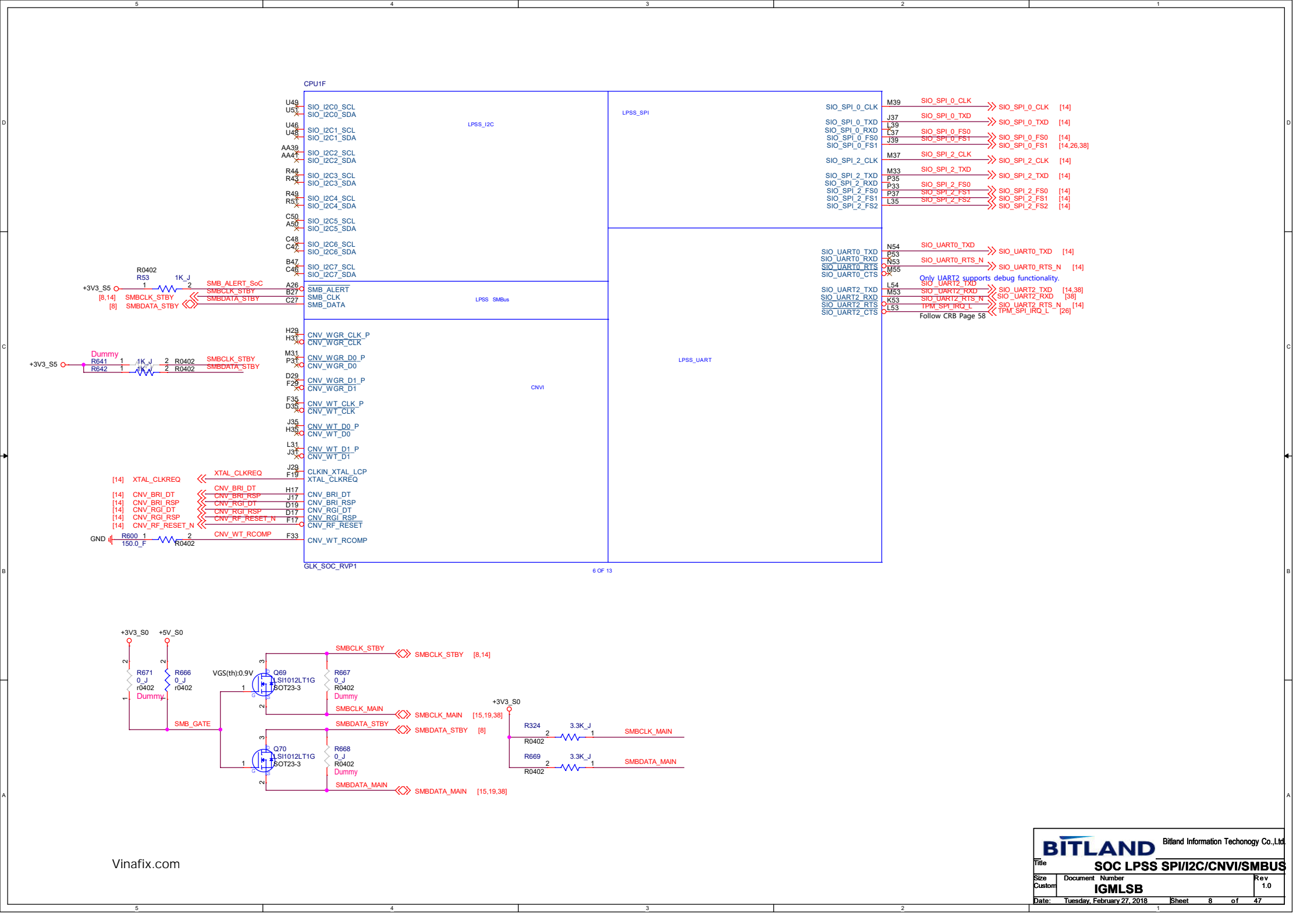


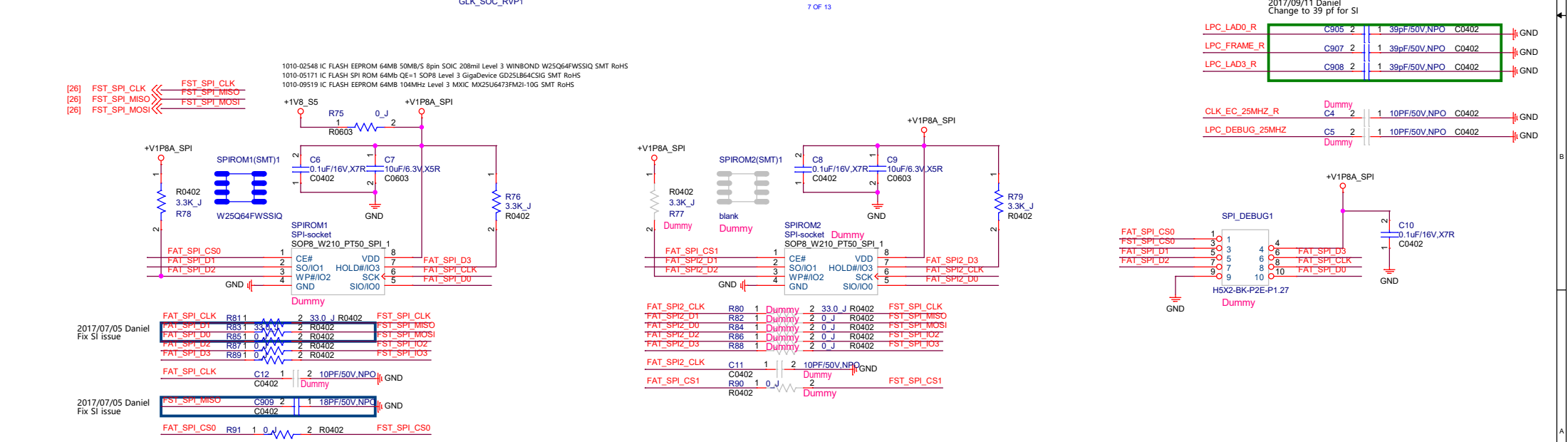
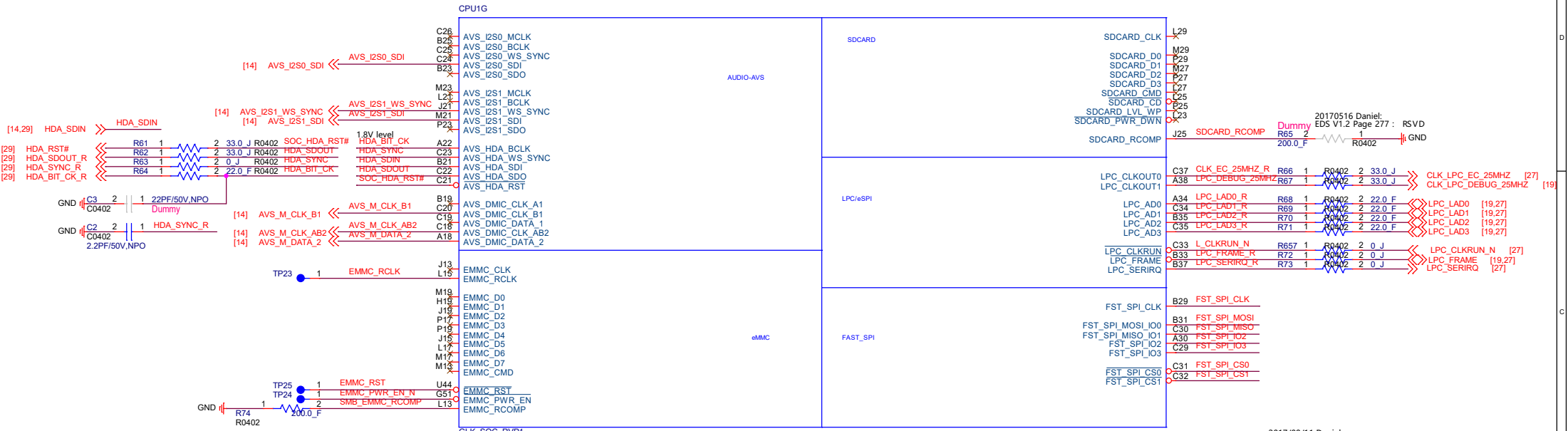
<b>BITLAND</b> Bitland Information Technology Co., Ltd.			
Title <b>SOC PCIe/USB/SATA</b>			
Size	Document	Number	Rev
Custom	<b>IGMLSB</b>		1.0
Date:	Tuesday, February 27, 2018	Sheet	6 of 47



20170721 Daniel:  
GP31=1, GP32=1, GP33= 1, QT:  
GP31=0, GP32=1, GP33= 1, YT:  
GP31=1, GP32=0, GP33= 1, A10330

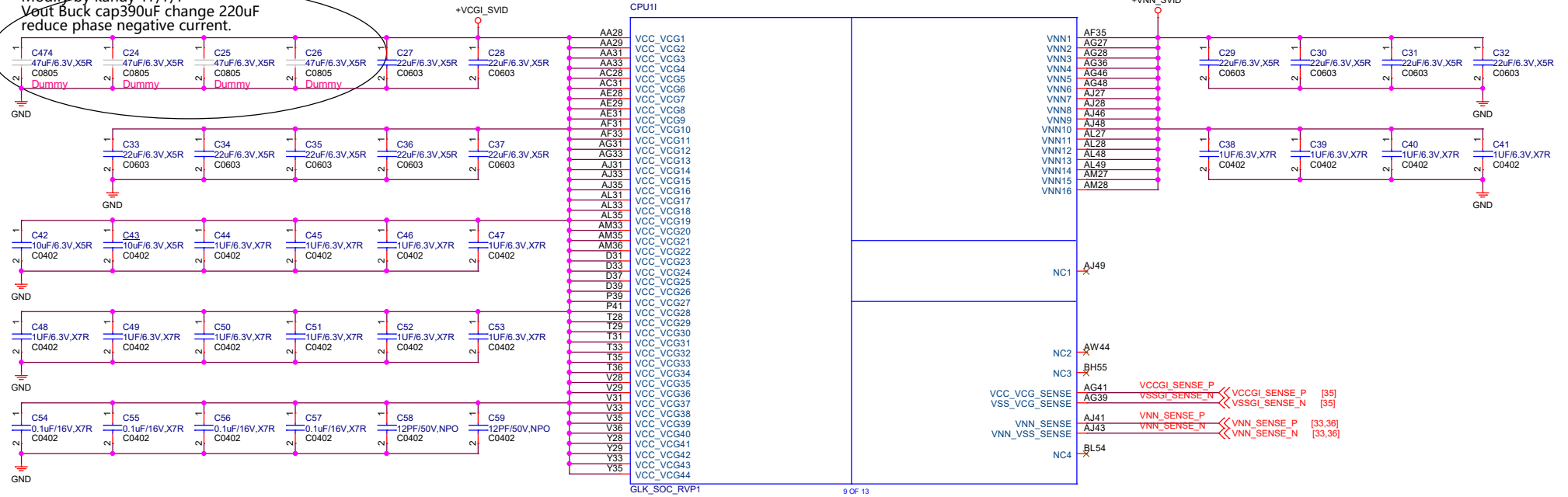
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GP31	1	0	1
GP32	1	1	1
GP33	1	1	1

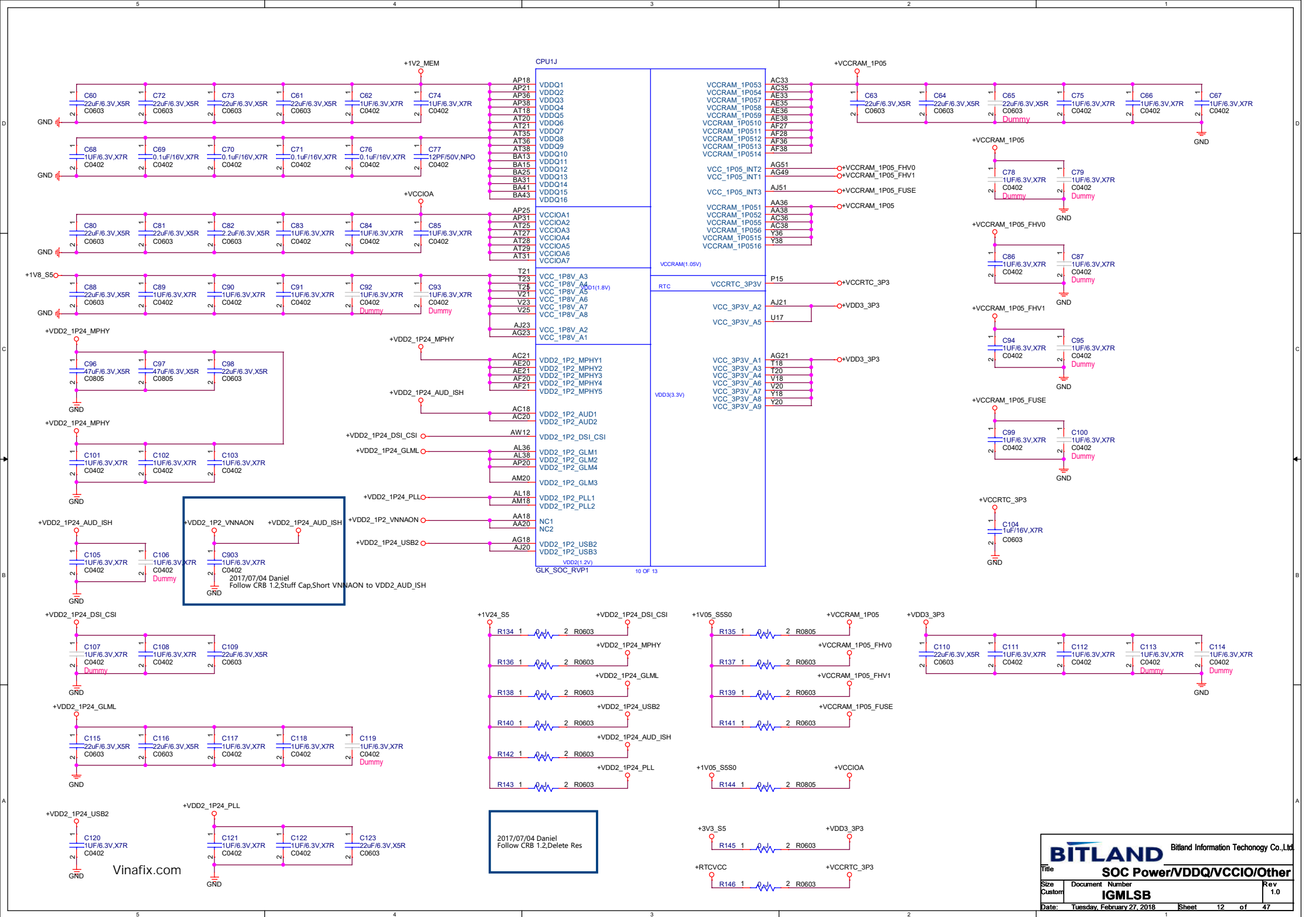


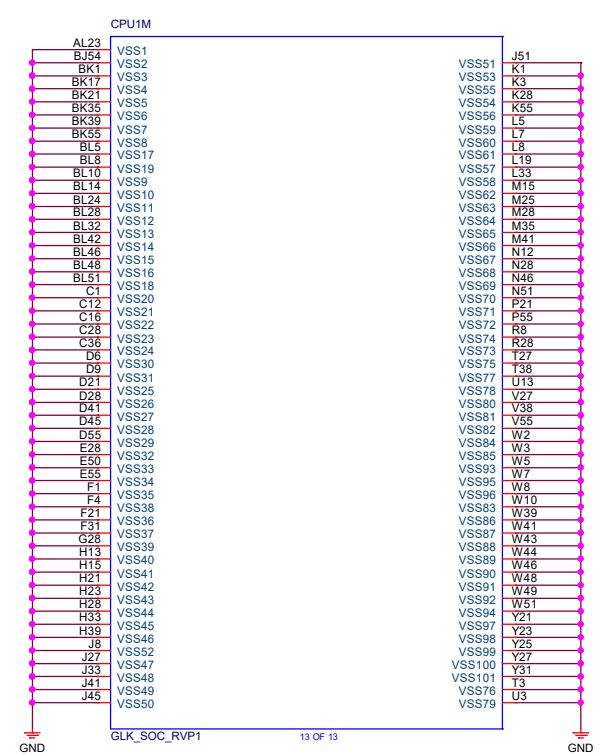
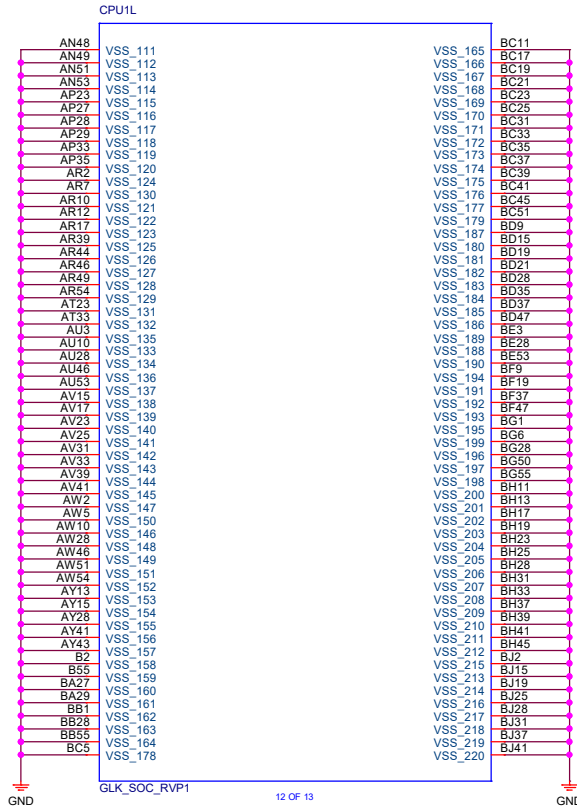
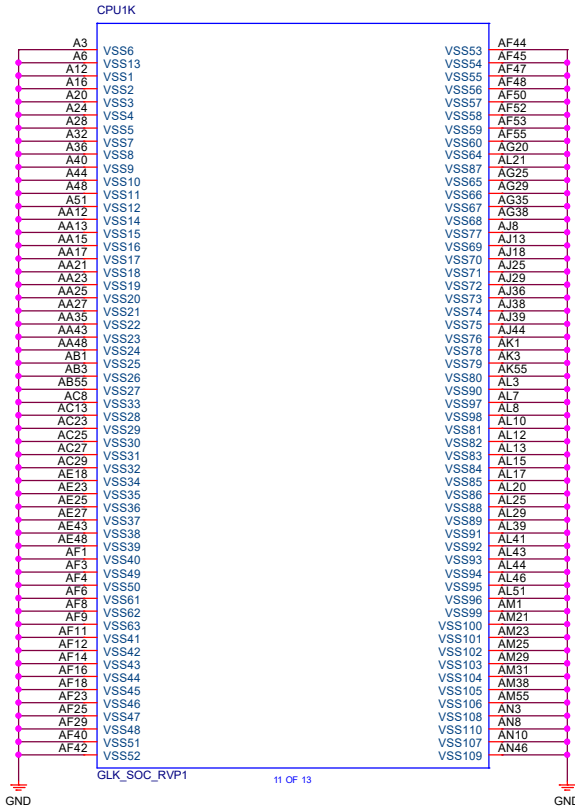




Modify by kandy 17/7/7  
 Vout Buck cap390uF change 220uF  
 reduce phase negative current.









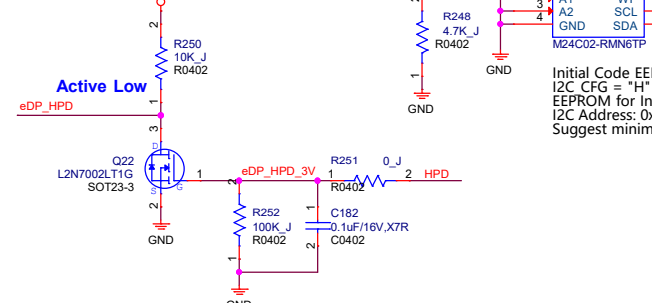
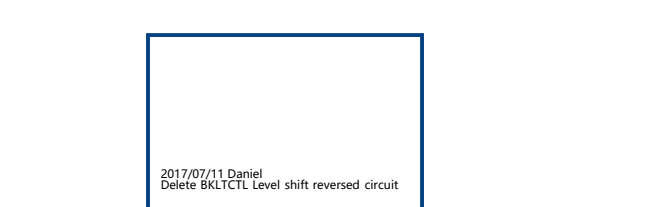
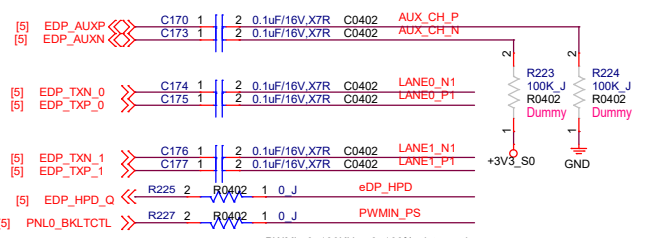
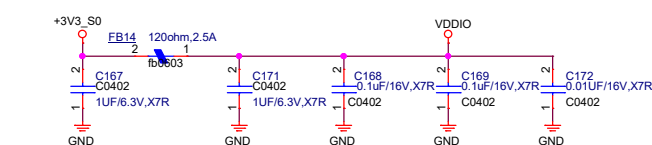
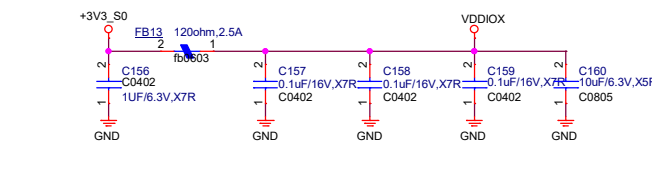
those straps is pulled HIGH when RSM\_RST\_N de-asserts for normal platform operation.

Flash Descriptor Override  
0 = No Override (Normal Operation)  
1 = Override  
Note: This strap enables the platform to override security features in the SPI.

MODE	SPI override
Normal	1-2
Override	2-3

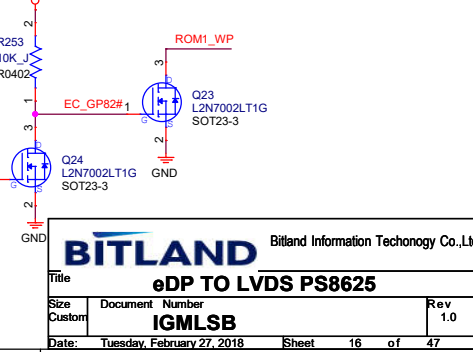
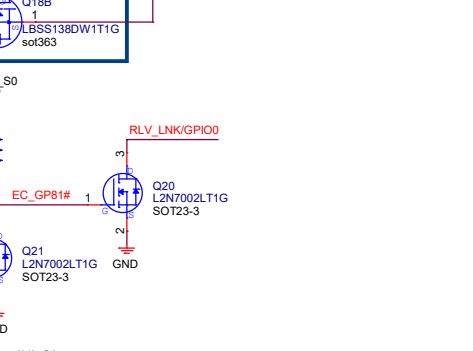
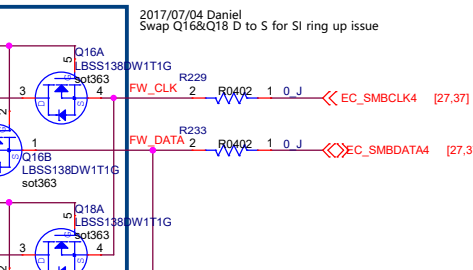
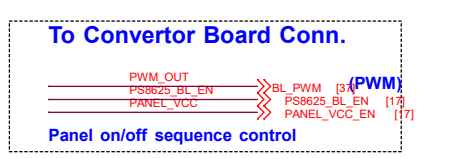
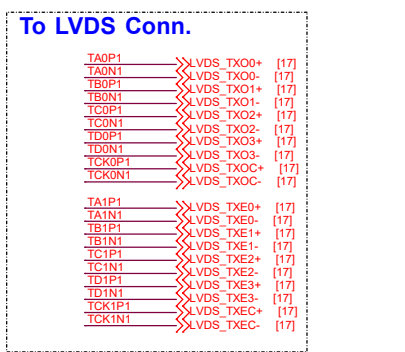
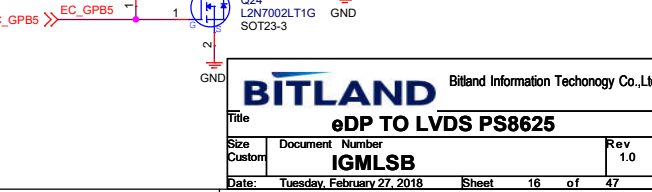
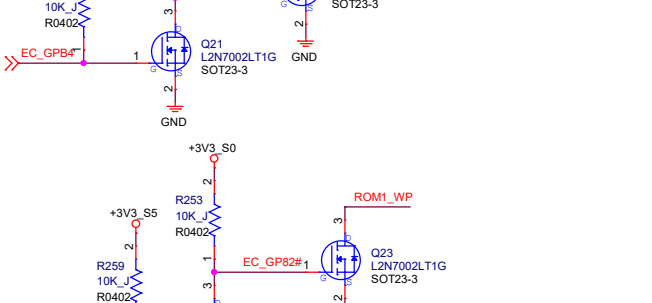
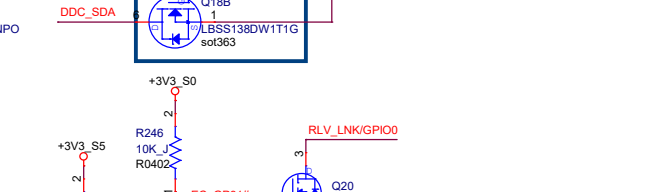
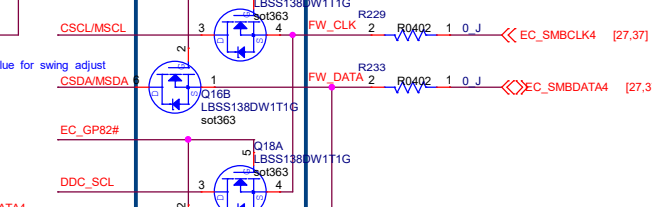
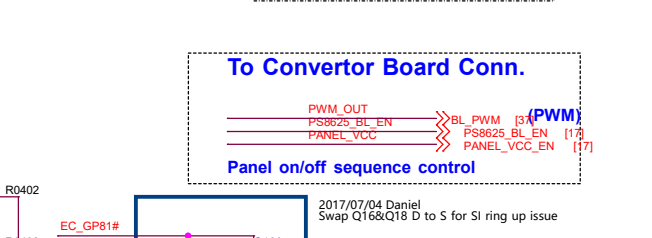
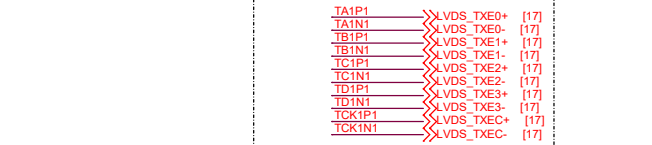
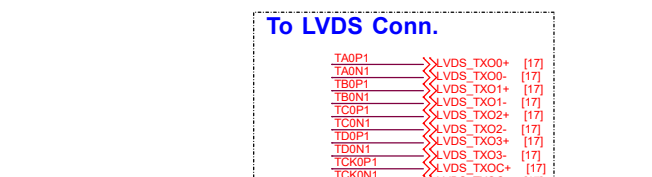
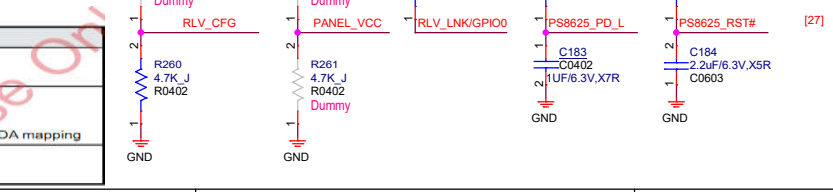
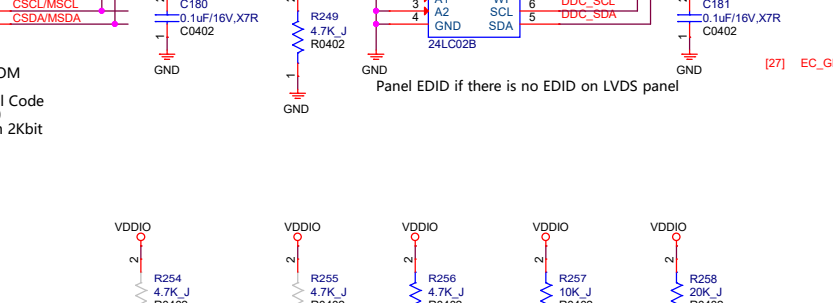
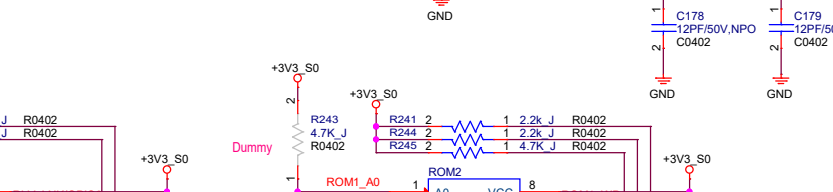
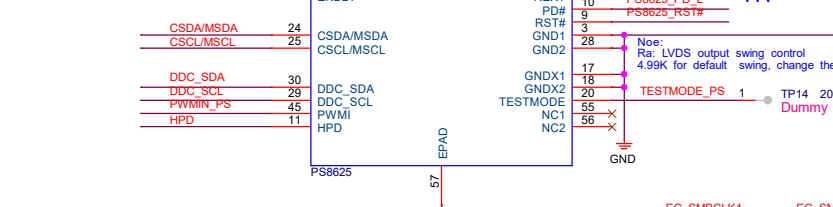
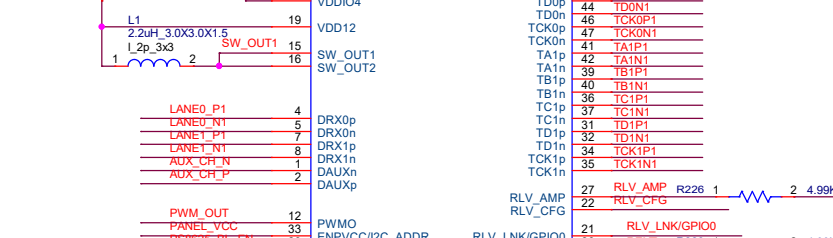
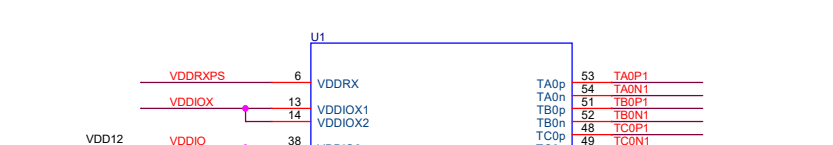
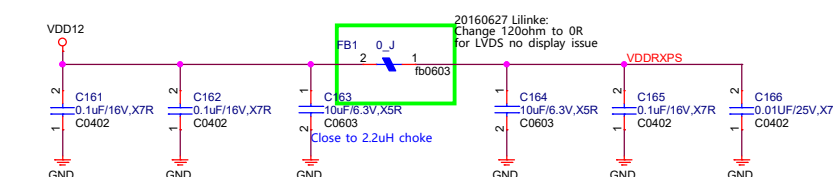
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AVS\_I2S1\_WS\_SYNC  
AVS\_I2S1\_SDI  
SMBCLK\_STBY  
CNV\_BRI\_RSP  
CNV\_RGI\_DT  
CNV\_RGI\_RSP  
CNV\_RF\_RESET\_N  
XTAL\_CLKREQ  
SIO\_UART0\_RTS\_N  
SIO\_SPI\_0\_CLK  
SIO\_SPI\_0\_FS0  
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SIO\_SPI\_2\_TXD

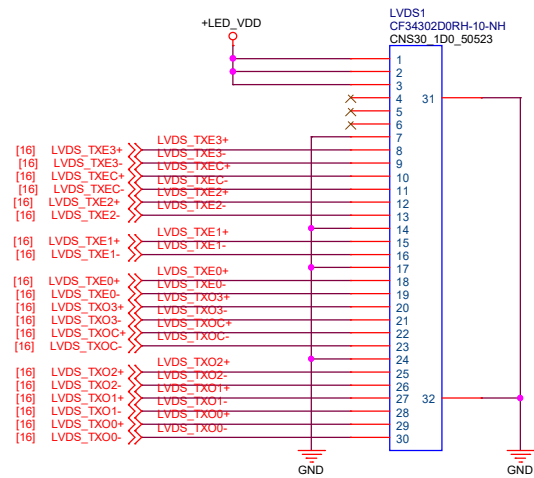




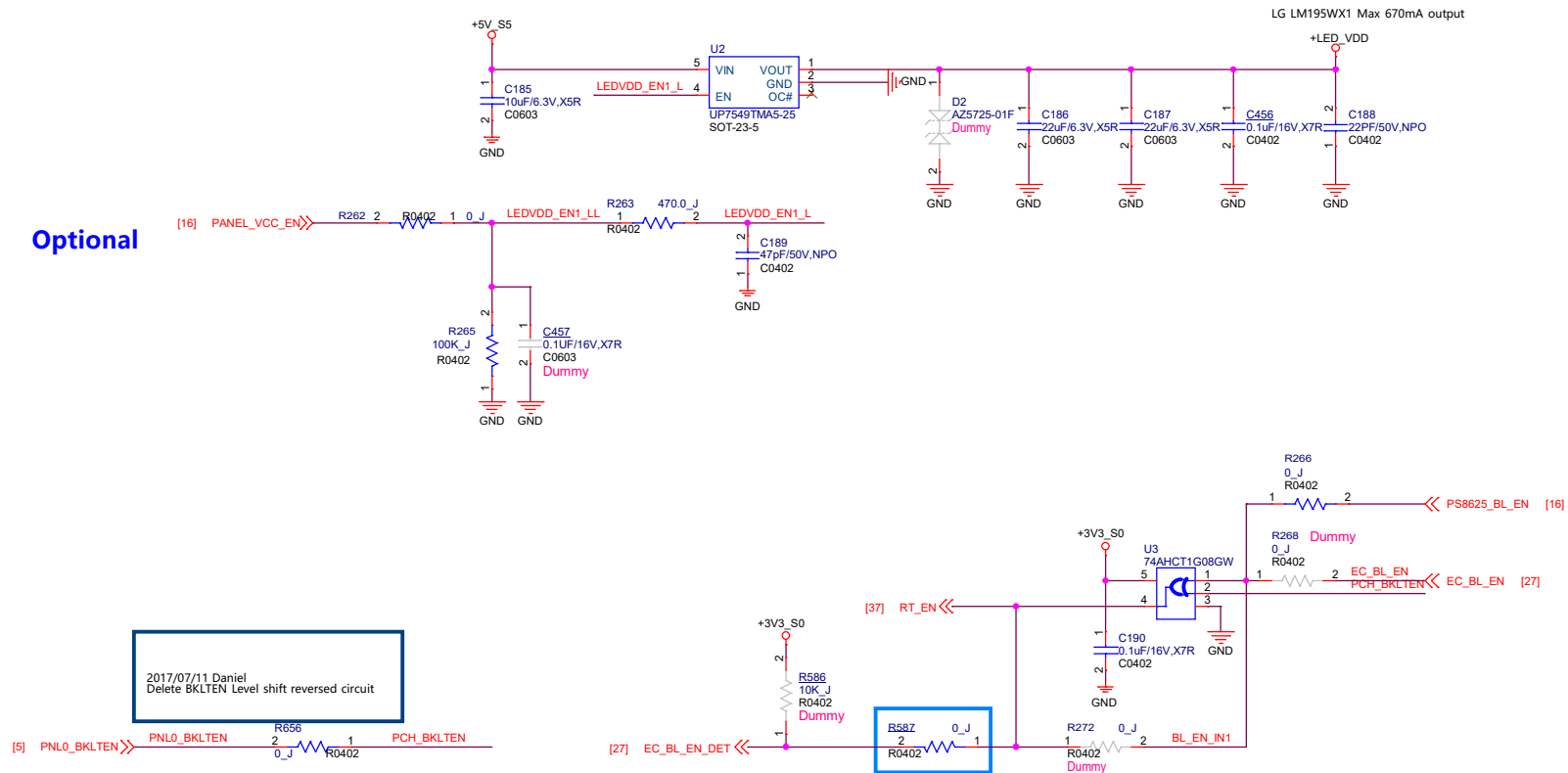
**Table11. Power on Pins Configuration**

Configuration Signal	Purpose	Definition
I2C_ADDR	I2C Slave address selection	L: 0x10h~0x1Fh H: 0x90h~0x9Fh
RLV_CFG	LVDS color depth and data selection	L: 8-bit LVDS, VESA mapping M: 8-bit LVDS, JEIDA mapping H: 6-bit LVDS, both VESA and JEIDA mapping
RLV_LNK	LVDS single link or dual link selection	L: Single link LVDS H: Dual link LVDS



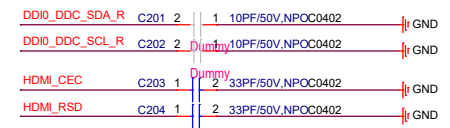
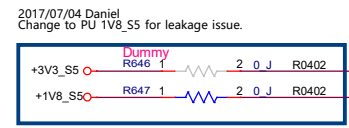
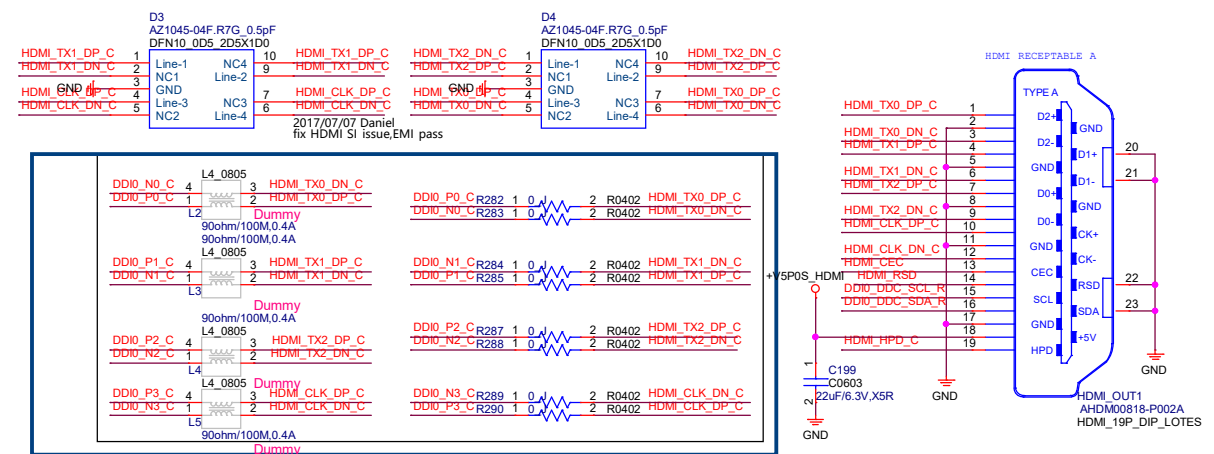


Optional

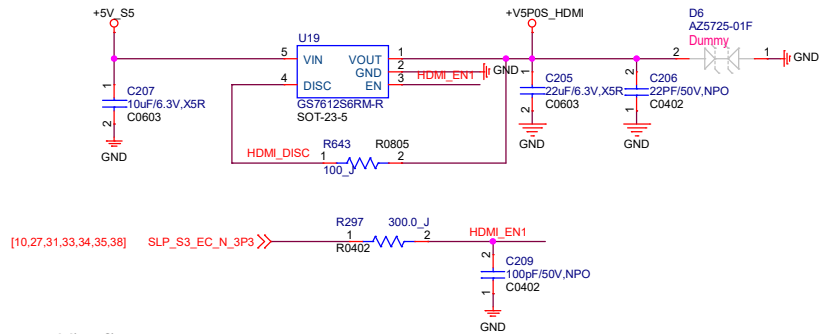
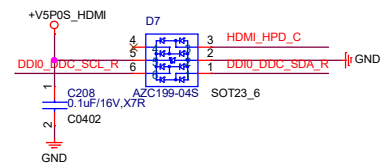


2017/07/11 Daniel  
Delete BKL TEN Level shift reversed circuit

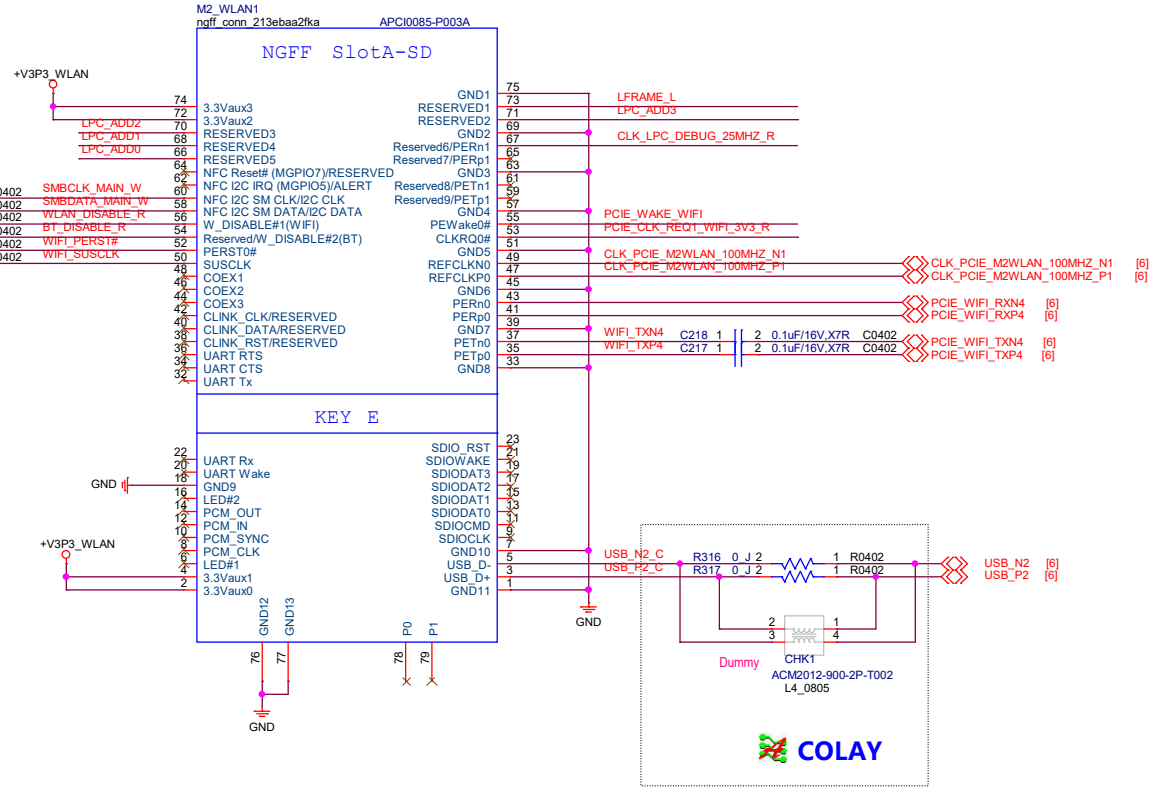
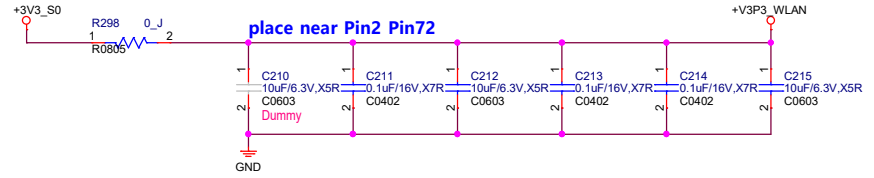
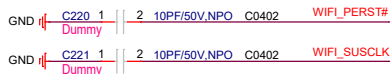
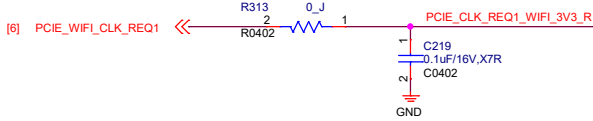
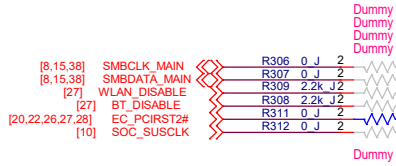
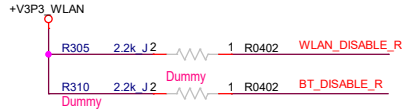
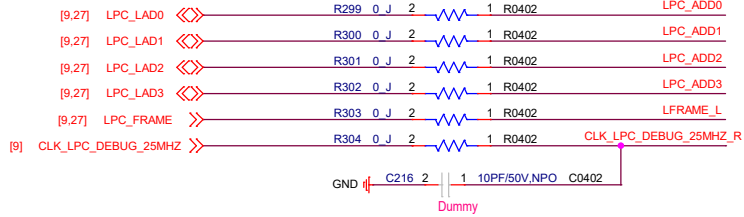
20160517 Liliinke:  
ADD PR203, 利 用 E C 的 GP 3 2 作为 G P I, 增加 S3 & R eboot 时 对 R T\_ E N

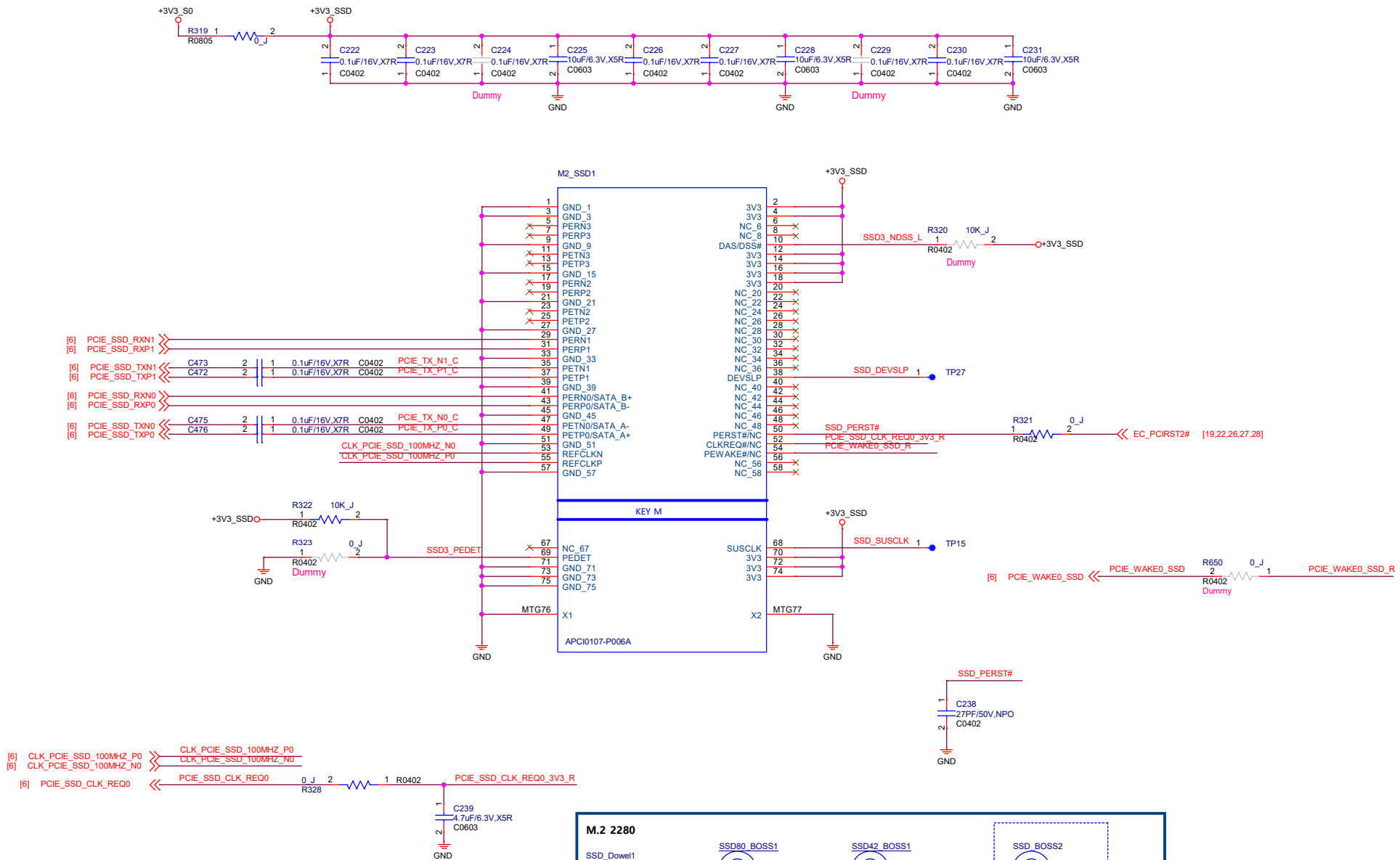


27	1'h0	<b>HV_DDI0_DDC_SCL</b> <b>(vccio_pad_hv_ddi0_ddc_scl):</b>  0 = PAD VCCIO is 3.3V <b>(default)</b> 1 = PAD VCCIO is 1.8V
26	1'h0	<b>HV_DDI0_DDC_SDA</b> <b>(vccio_pad_hv_ddi0_ddc_sda):</b>  0 = PAD VCCIO is 3.3V <b>(default)</b> 1 = PAD VCCIO is 1.8V

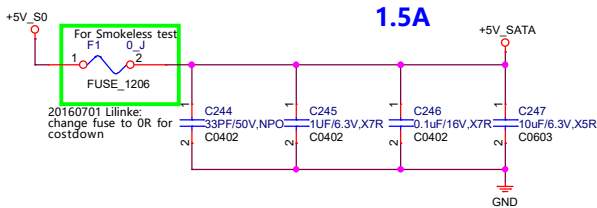


## For Debug Card

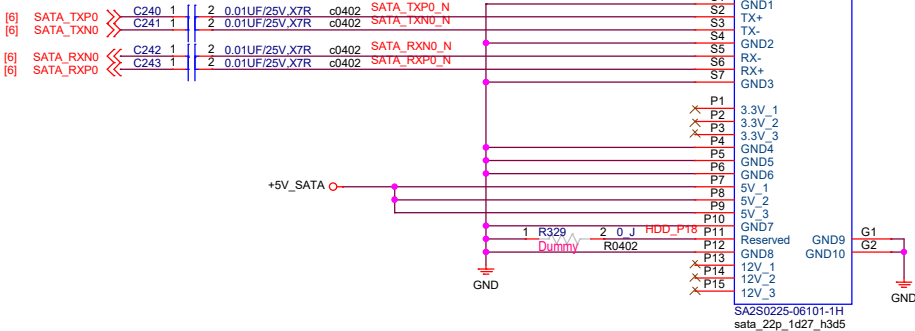




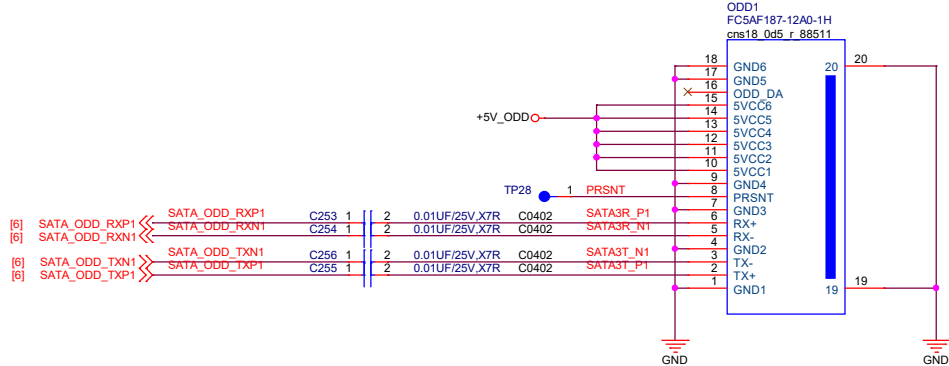
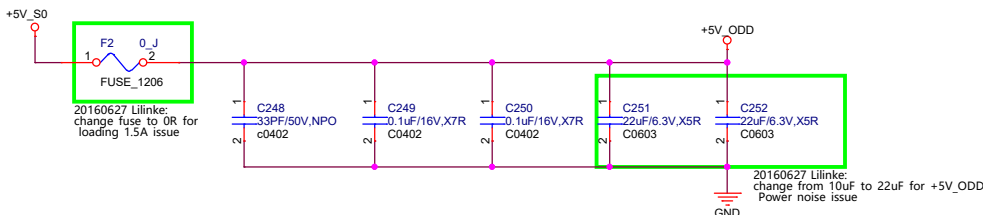
SATA HDD CONN



SATA 3.0 CONN



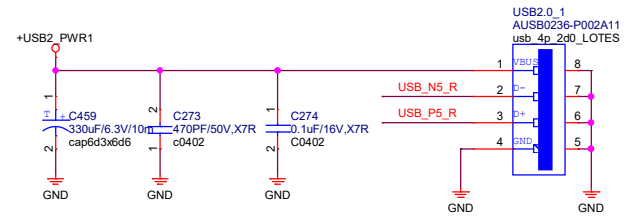
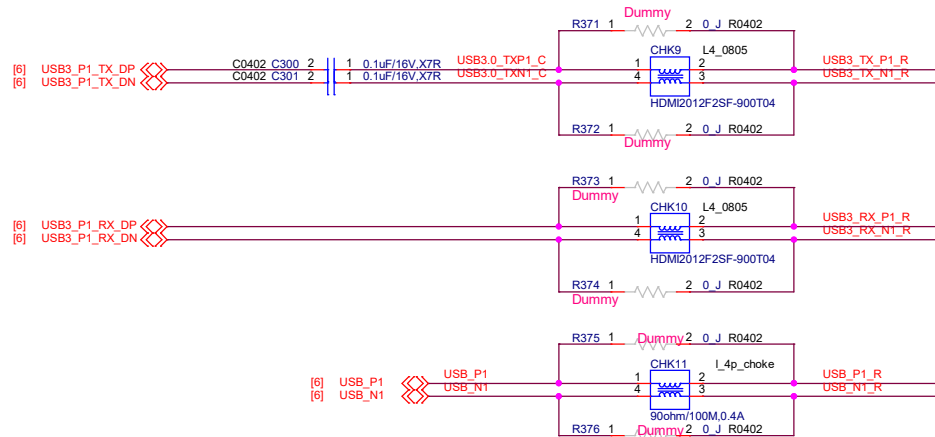
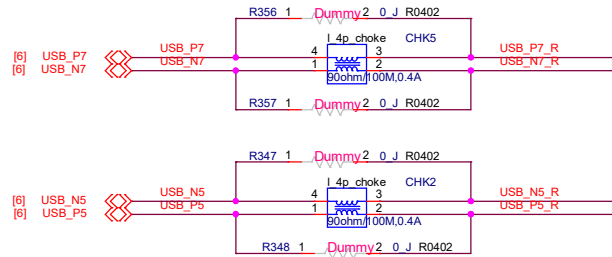
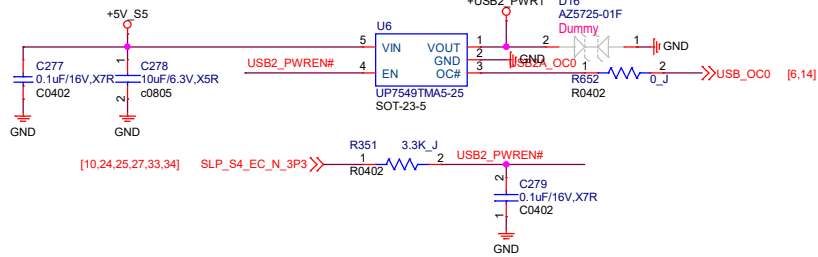
SATA ODD CONN



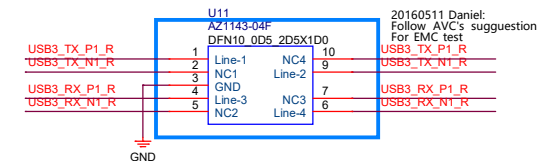
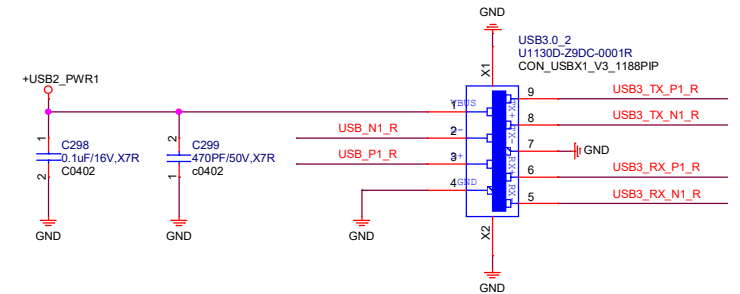
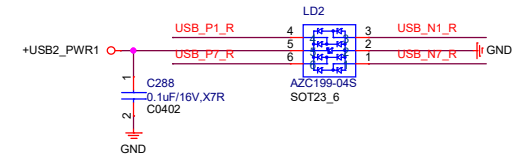
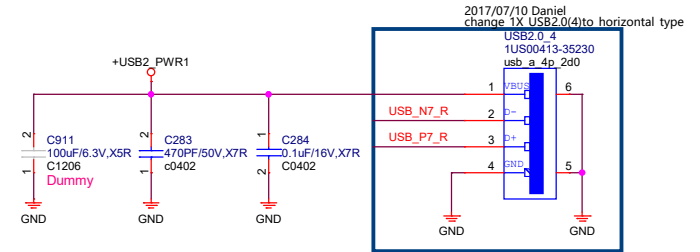
PIN DEFINE	CONN	FFC
GND	P6	18
GND	P5	17
ODD_DA	P4	16
5V	P2/P3	15
5V		14
5V		13
5V		12
5V		11
5V		10
5V		9
PRSNT	P1	8
GND	S7	7
RXP	S6	6
RXN	S5	5
GND	S4	4
TXN	S3	3
TXP	S2	2
GND	S1	1

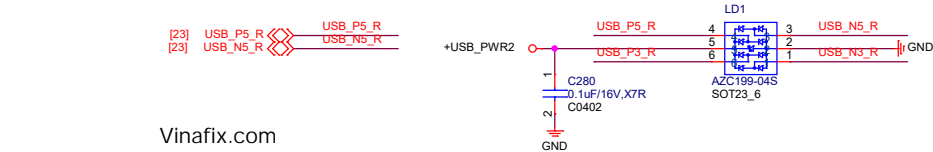
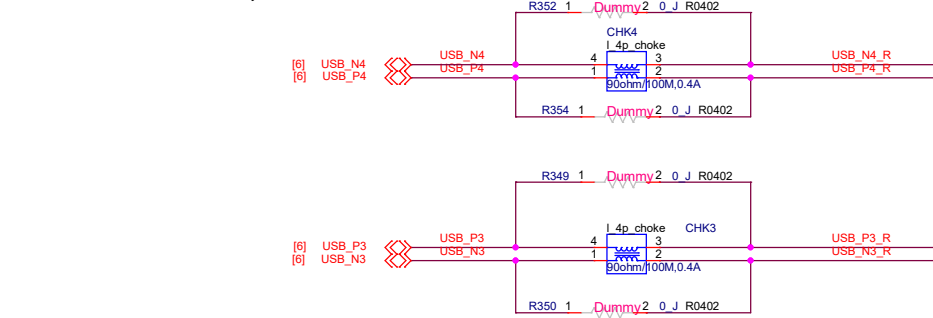
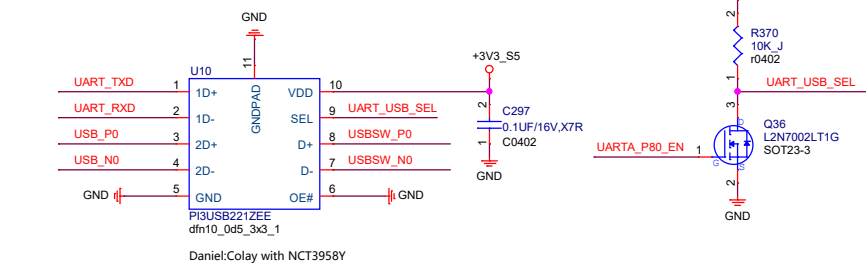
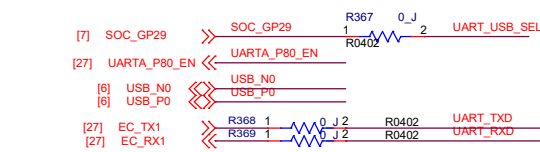
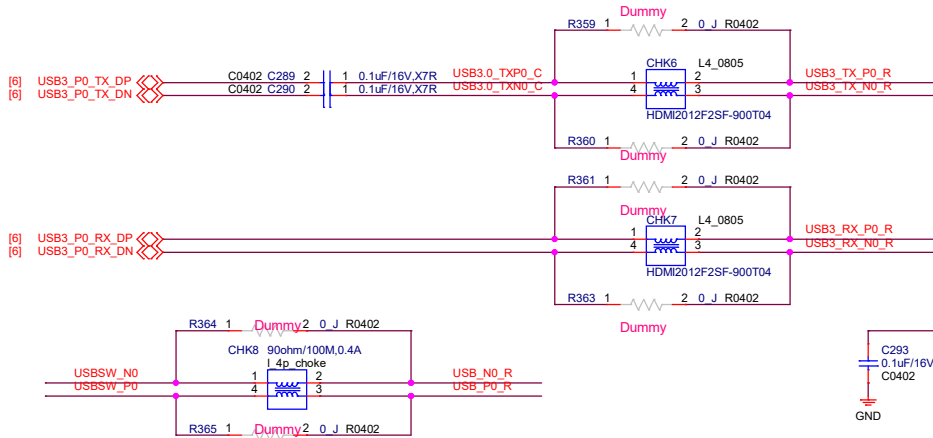
8组线位 31个点





2017/07/11 Daniel  
USB2.0\_1, USB2.0\_4, USB3.0\_2 use common load switch and cap



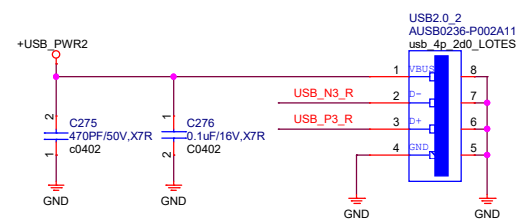
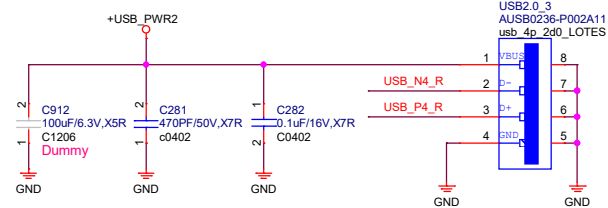
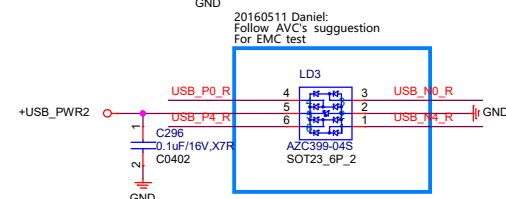
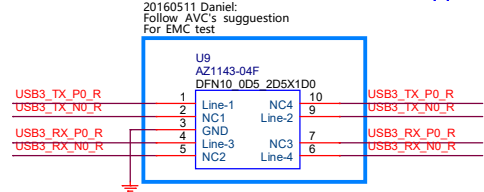
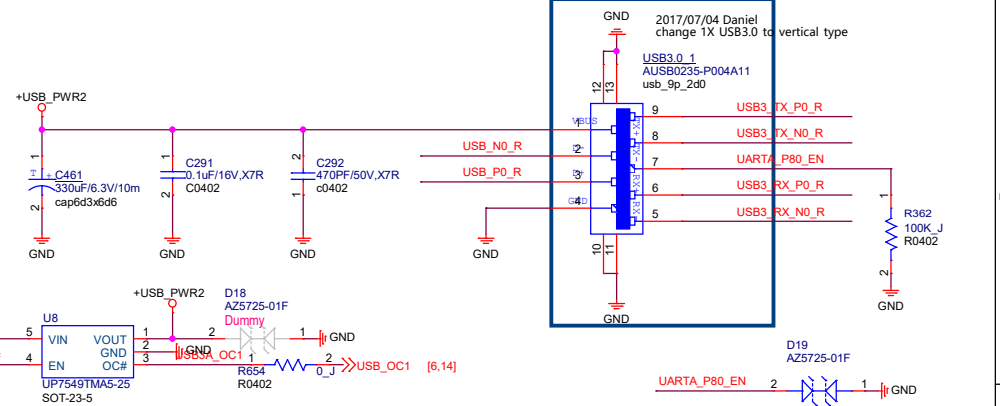


OE#	S	Function
H	X	Disable
L	L	To 1D
L	H(Default)	To 2D

PCH_GPIO_D16	kernel debug
Set input	disable
set output low	enable

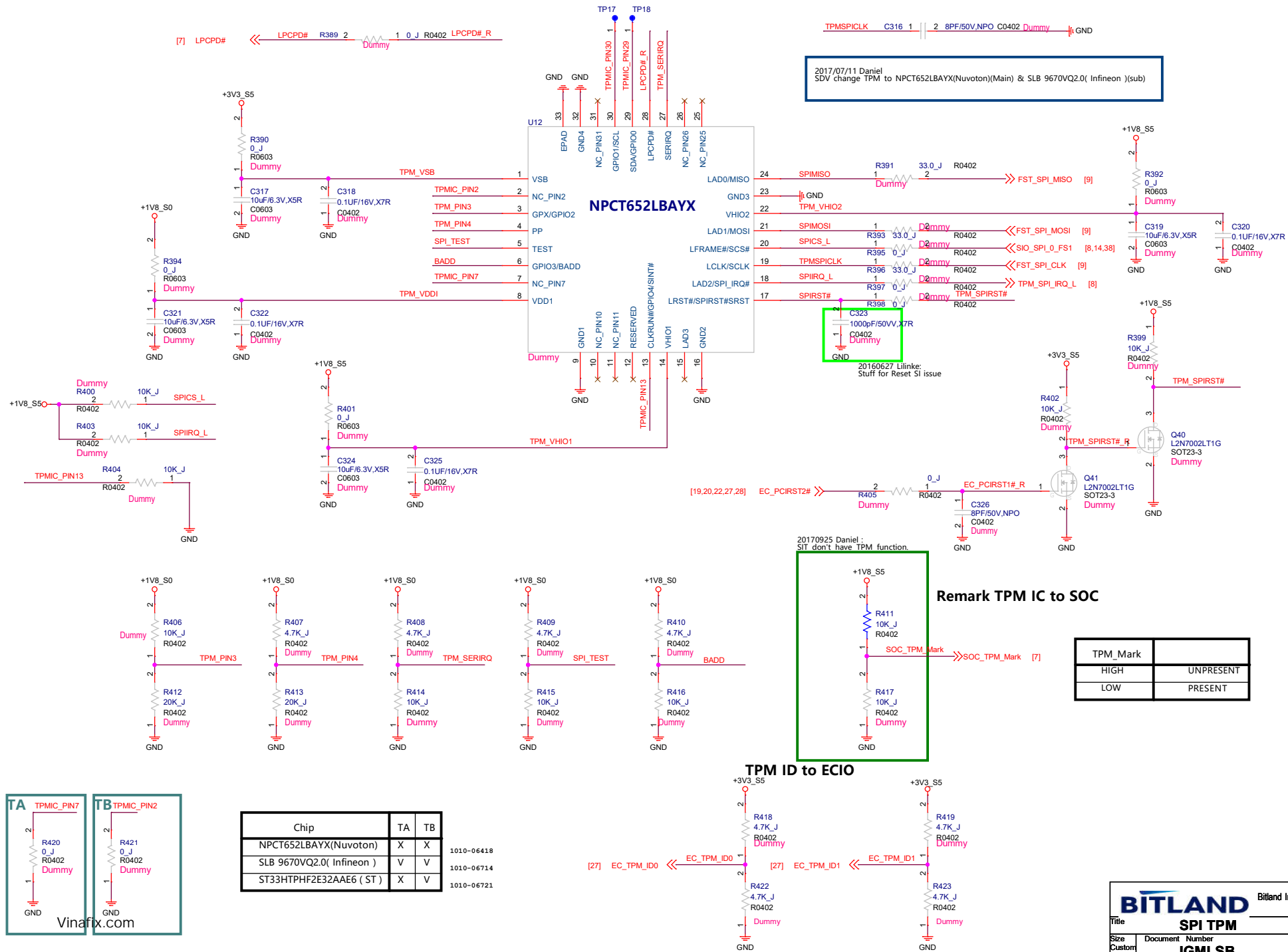
UARTA_P80_EN	Post 80
L	disable
H	enable

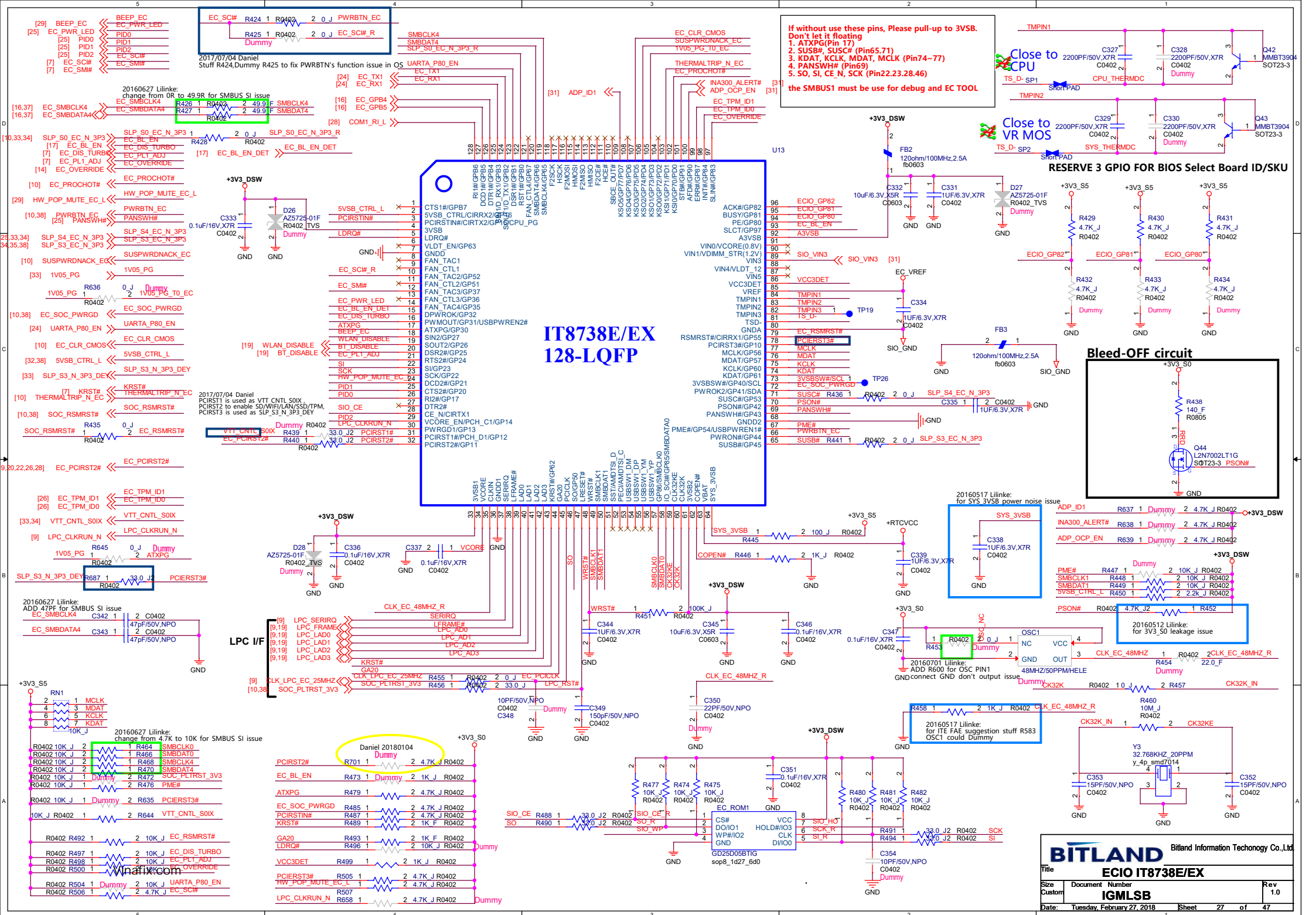
2017/07/11 Daniel  
USB3.0\_1,USB2.0\_3,USB2.0\_2 use common load switch and cap

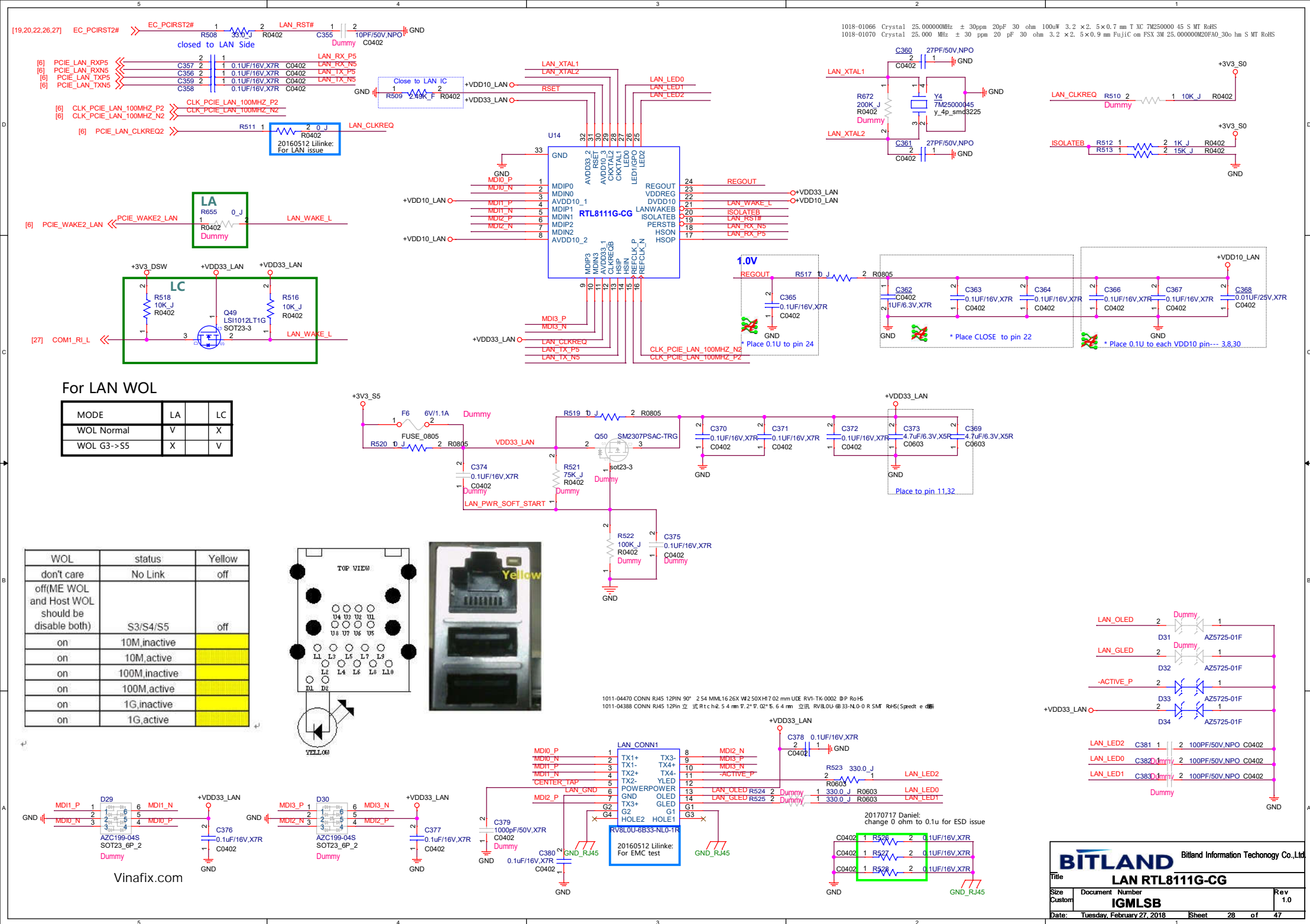


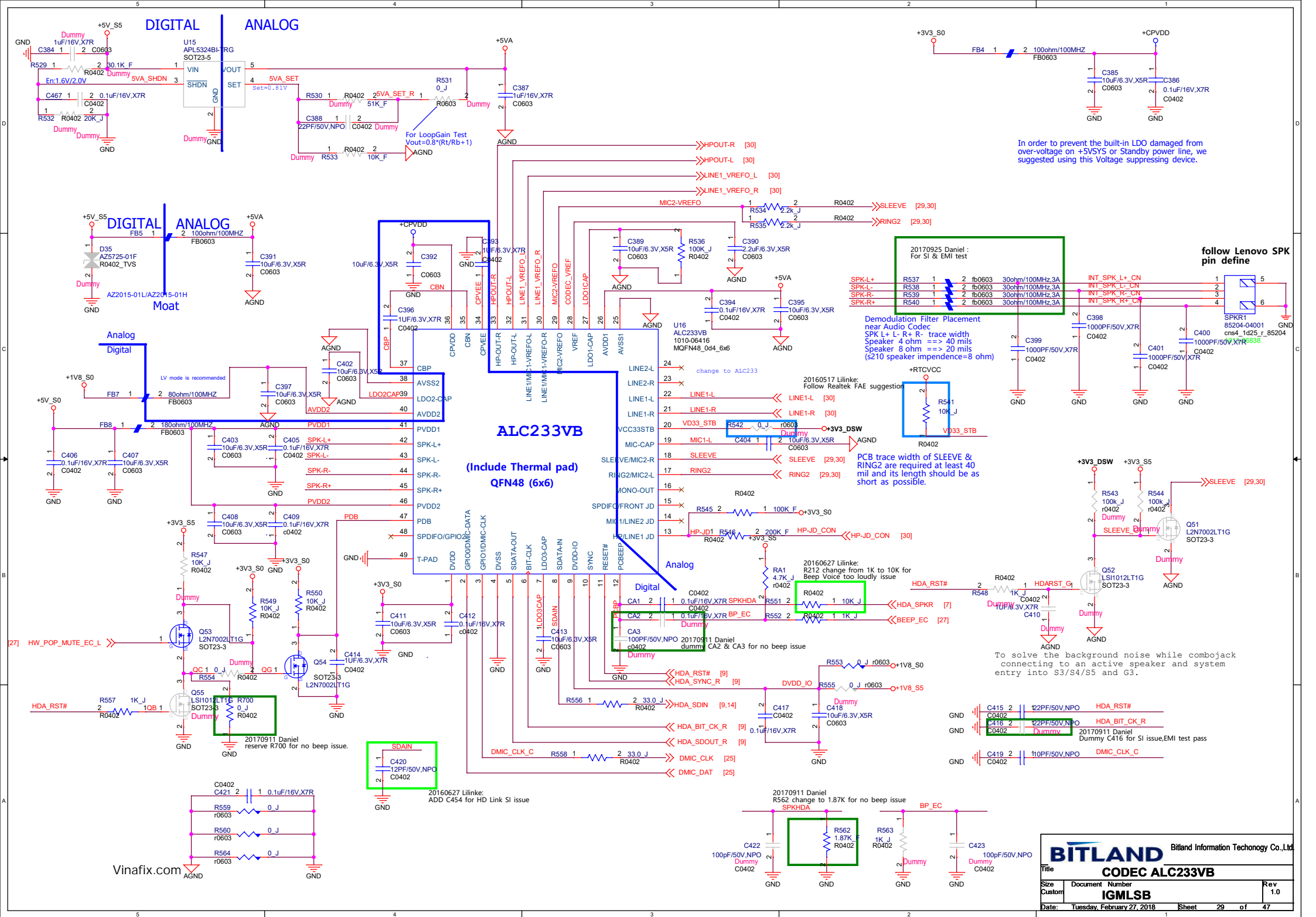


TPM Circuit(1.8V)









In order to prevent the built-in LDO damaged from over-voltage on +5V<sub>VSYS</sub> or Standby power line, we suggested using this Voltage suppressing device.

20170925 Daniel : For SI & EMI test

Demodulation Filter Placement near Audio Codec  
SPK L+ L- R+ R- trace width  
Speaker 4 ohm ==> 40 mils  
Speaker 8 ohm ==> 20 mils  
(s210 speaker impedance=8 ohm)

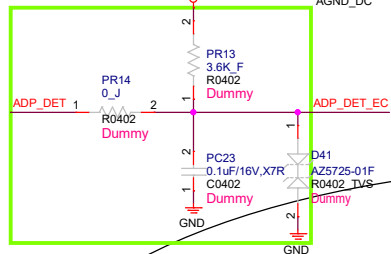
PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 and G3.

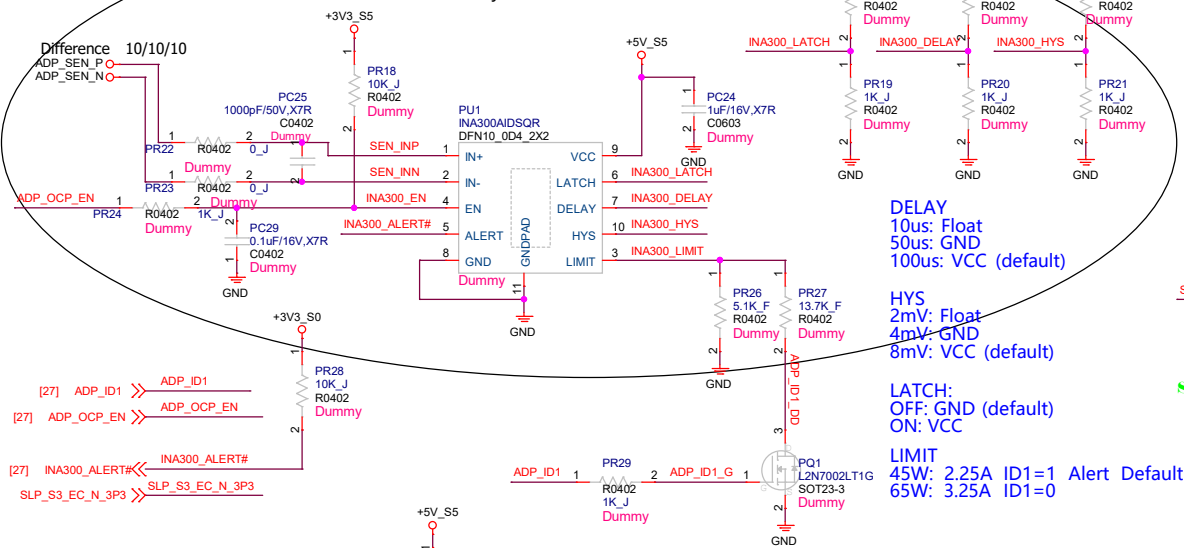


# DC IN

2017/08/10 Daniel  
Change to dummy, no function



Modify by kandy 17/7/7  
Dummy OBP circuit



DELAY  
10us: Float  
50us: GND  
100us: VCC (default)

HYS  
2mV: Float  
4mV: GND  
8mV: VCC (default)

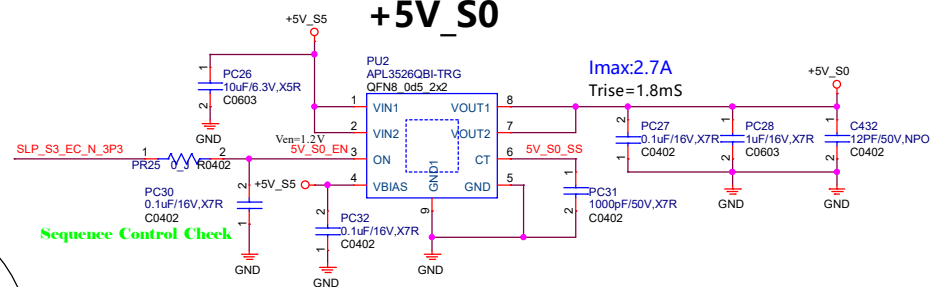
LATCH:  
OFF: GND (default)  
ON: VCC

LIMIT  
45W: 2.25A ID1=1 Alert Default  
65W: 3.25A ID1=0

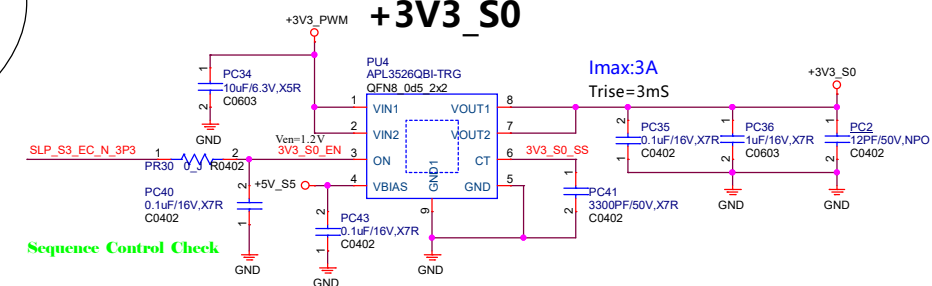
2017/08/10 Kandy  
Change to Short Pad



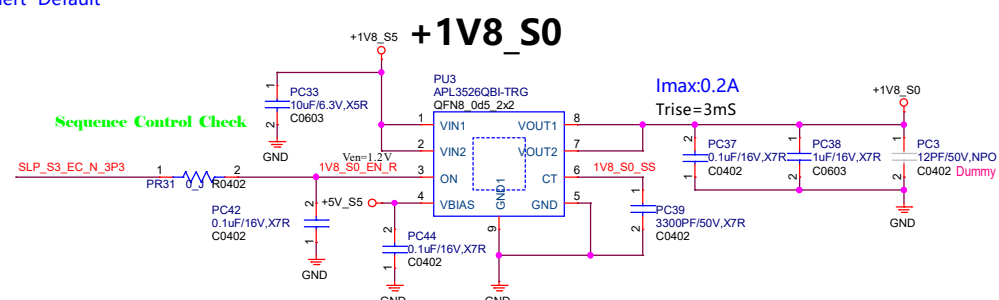
## +5V\_S0



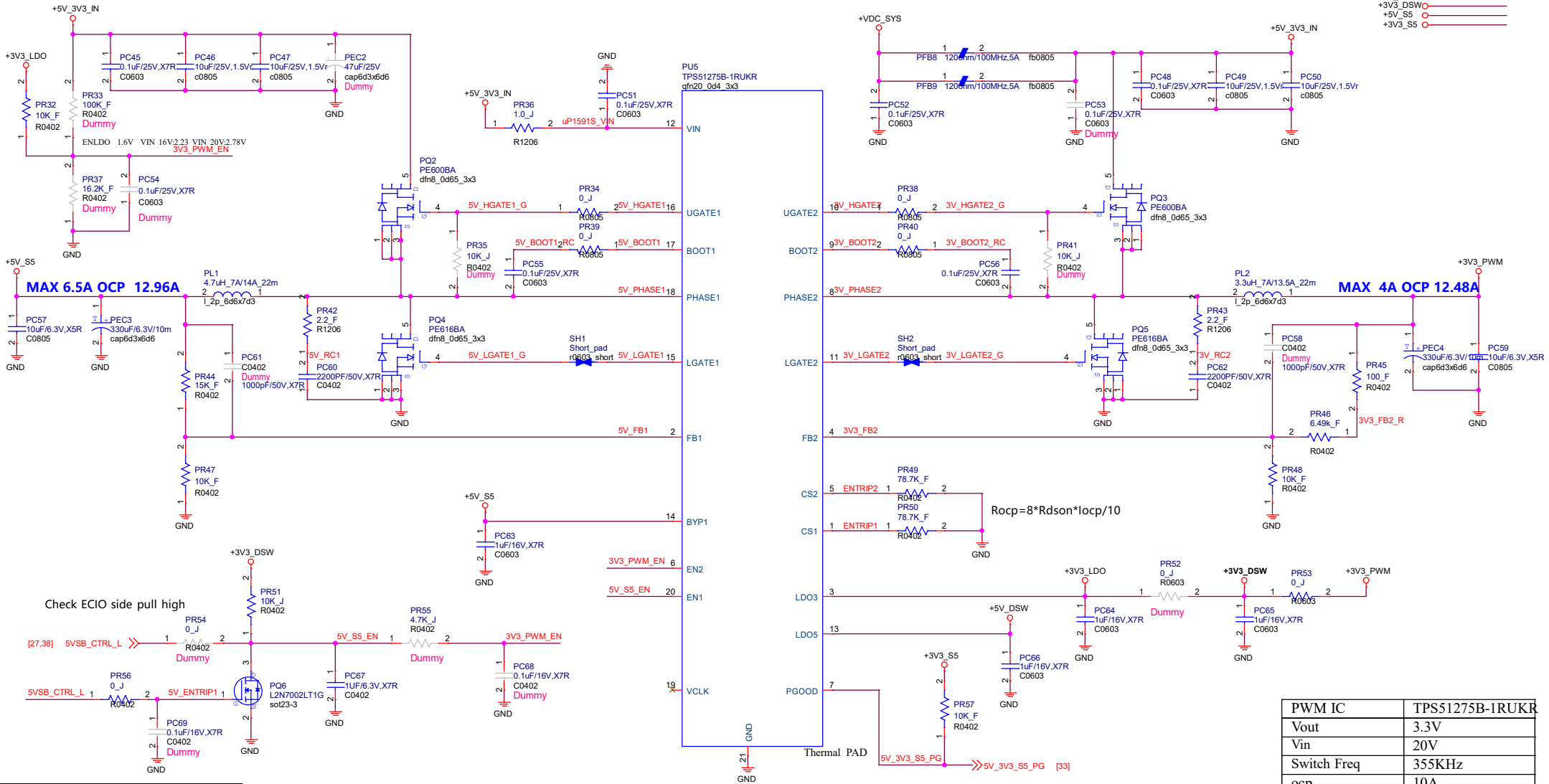
## +3V3\_S0



## +1V8\_S0



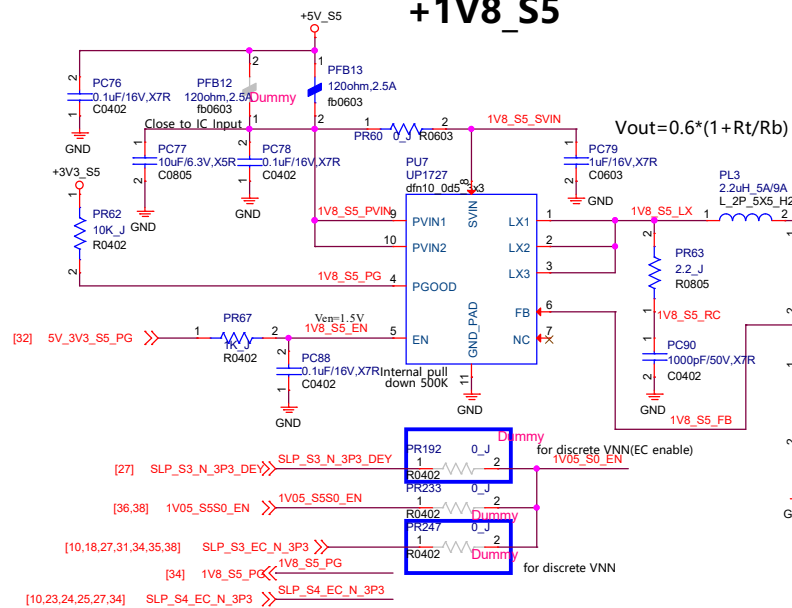
# +5V\_S5/+3V3\_S5



PWM IC	TPS51275B-1RUKR
Vout	5V
Vin	20V
Switch Freq	300KHz
ocp	10A
MLCC_Iripple	10uF/1A,47uF/2.5A
Choke size	4.7uH/7.3x6.8mm
Choke Idc/Isat	7A/10A
Choke DCR	22mΩ
Cin CAP	20.1uF+47uF
Cout CAP	330uF
Cout CAP_ESR	10mΩ
LIR	0.2-0.4

PWM IC	TPS51275B-1RUKR
Vout	3.3V
Vin	20V
Switch Freq	355KHz
ocp	10A
MLCC_Iripple	10uF/1A,47uF/2.5A
Choke size	3.3uH/7.3x6.8mm
Choke Idc/Isat	7A/10A
Choke DCR	22mΩ
Cin CAP	20.1uF+47uF
Cout CAP	330uF
Cout CAP_ESR	15mΩ
LIR	0.2-0.4

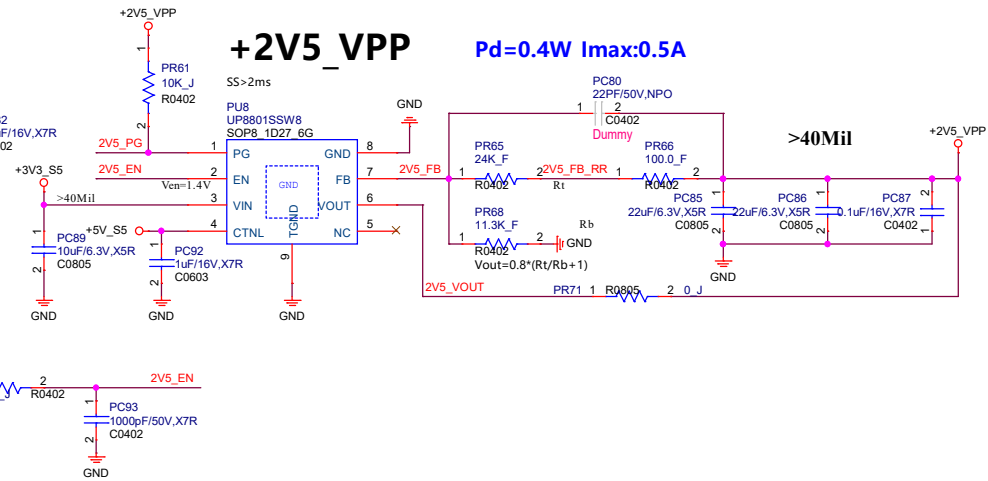
## +1V8\_S5



1.8V MAX 2A OCP 6.12A >80mV

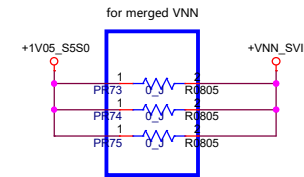
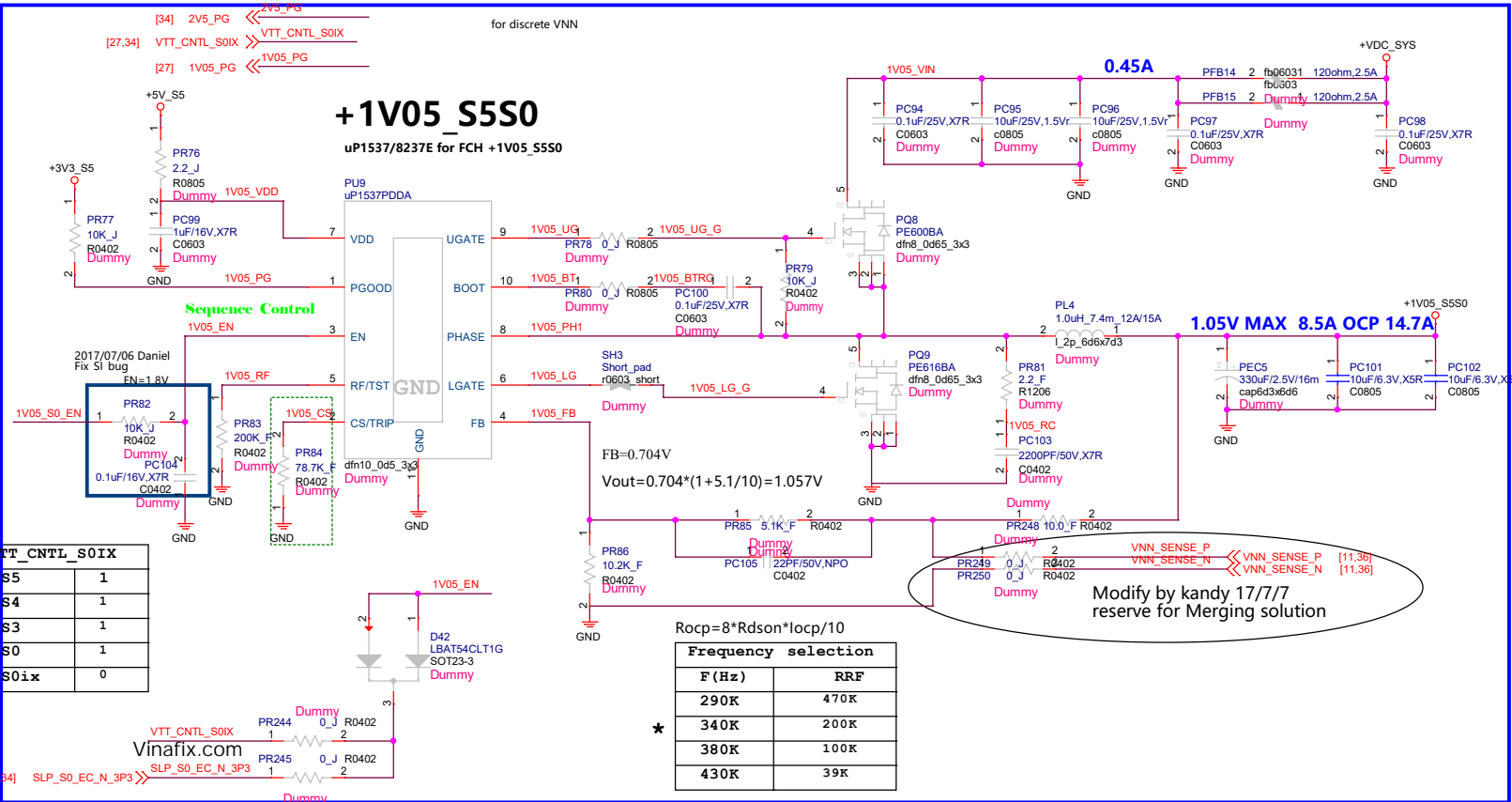
## +2V5\_VPP

$P_d = 0.4W$   $I_{max} = 0.5A$



## +1V05\_S5S0

uP1537/8237E for FCH +1V05\_S5S0



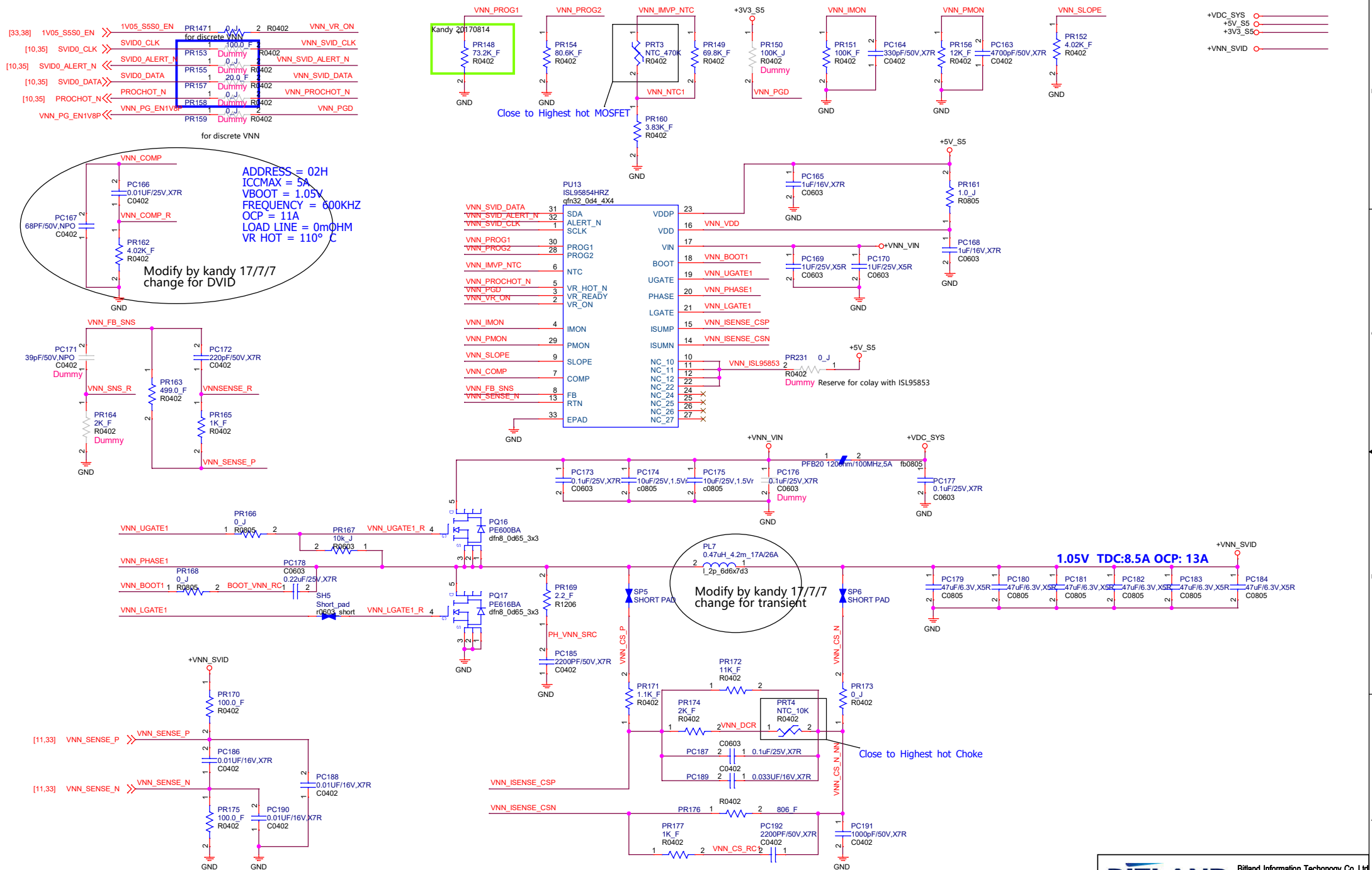
PWM IC	uP1537P/RT8237E
Vout	1.05V
Vin	20V
Switch Freq	340KHz
ocp	14A
MLCC_Iripple	10uF/1A
Choke size	1.0uH/7.3x6.8mm
Choke Idc/Isat	12A/15A
Choke DCR	7.4mΩ
Cin CAP	20.1uF
Cout CAP	330uF
Cout CAP_ESR	17mΩ
LIR	0.2-0.4



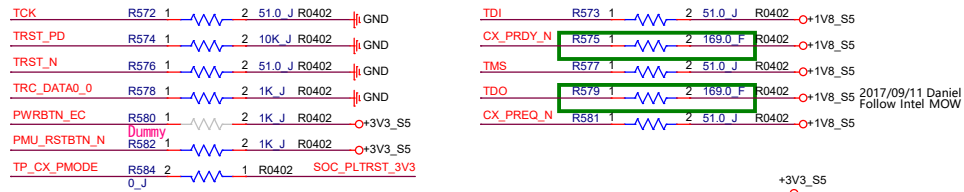


PROG1: Iccmax=8A for Merged;  
VNN(02h),

PROG2: SW Freq = 600kHz,  
VID fast slew rate = 32mV/us, Vboot=1.05V







## L2N7002LT1G $V_{GS(th)}$

1007-00362 MOSFET N- Channel 60V  $\pm 20V1$ .  $\theta_V \pm 1.15mA1$ .  $8\Omega @V$  2.25mWSOT-23 SMT LRC L2N7002LT1G BHS

### ON CHARACTERISTICS (Note 2.)

Gate Threshold Voltage  
( $V_{DS} = V_{GS}$ ,  $I_D = 250 \mu A$ )

$V_{GS(th)}$	1.0	1.6	2	$V_{dc}$
--------------	-----	-----	---	----------

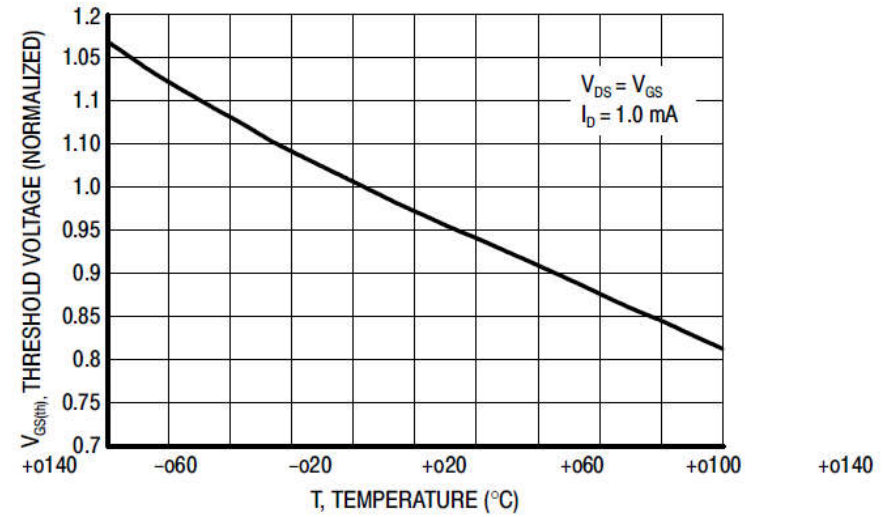


Figure 4. Temperature versus Gate Threshold Voltage

## NX3008NBK $V_{GS(th)}$ :Max 1.1V

1007-00468 MOSFET N-CH VDS:30V VGS:8V  $V_{GS(th)}$ typ:0.9V  $I_D$ :0.4A  $1.4\Omega$  @ 5V S OT-23 S M NXP NX3008 NBK RoHS

$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25^\circ C$	0.6	0.9	1.1	V
--------------	-------------------------------	--	-----	-----	-----	---

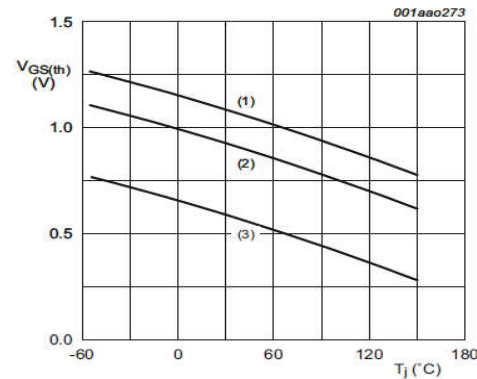
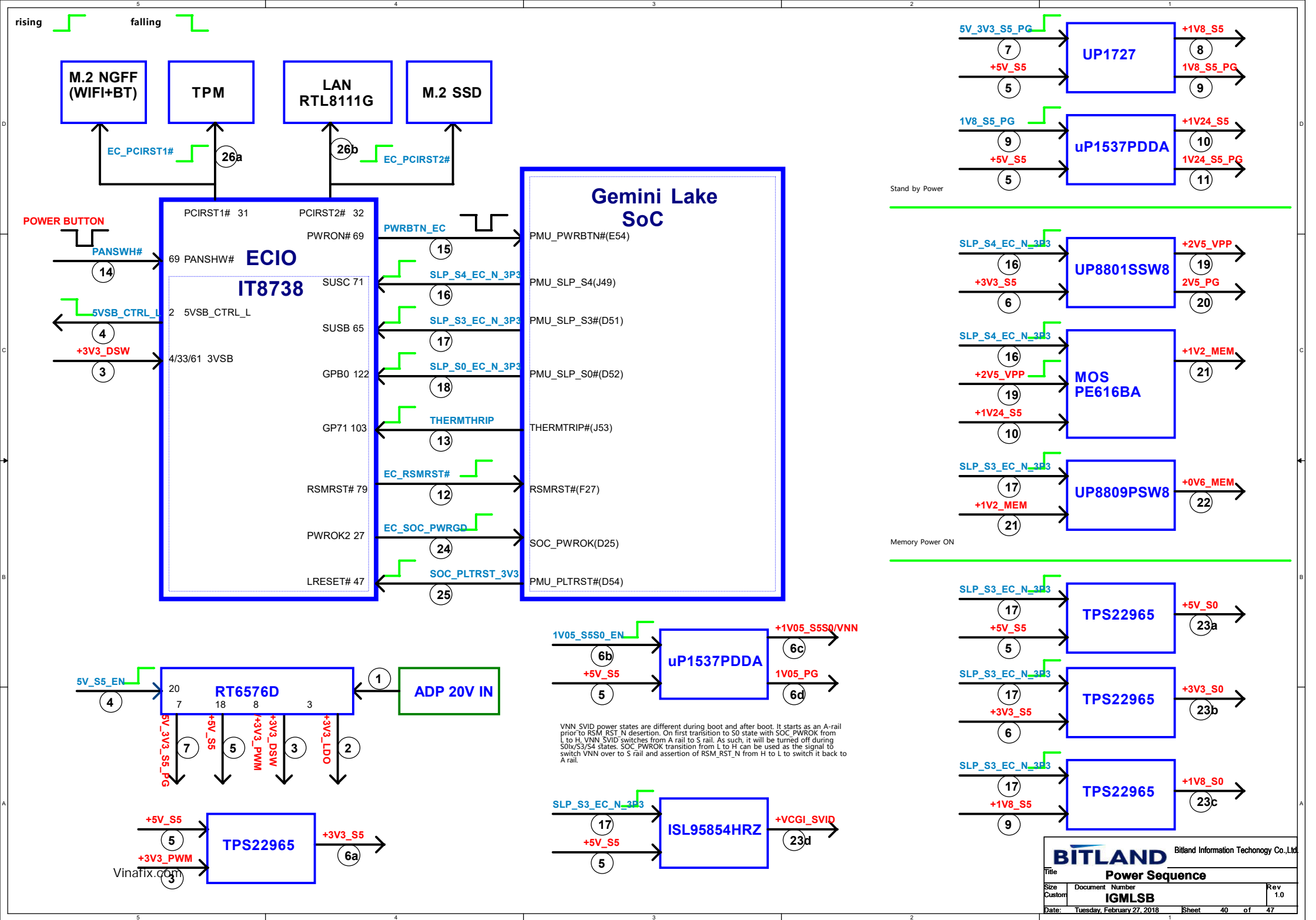
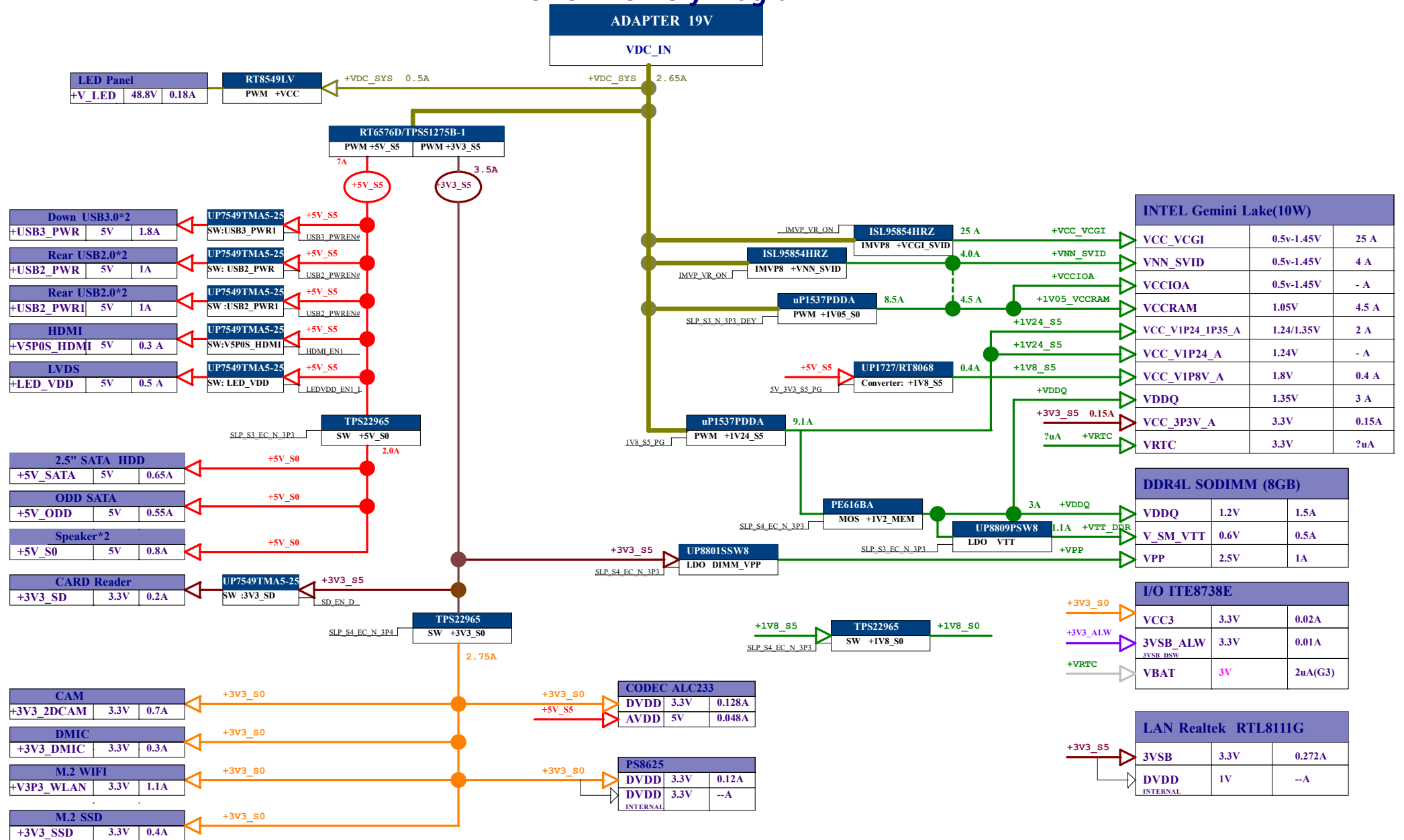


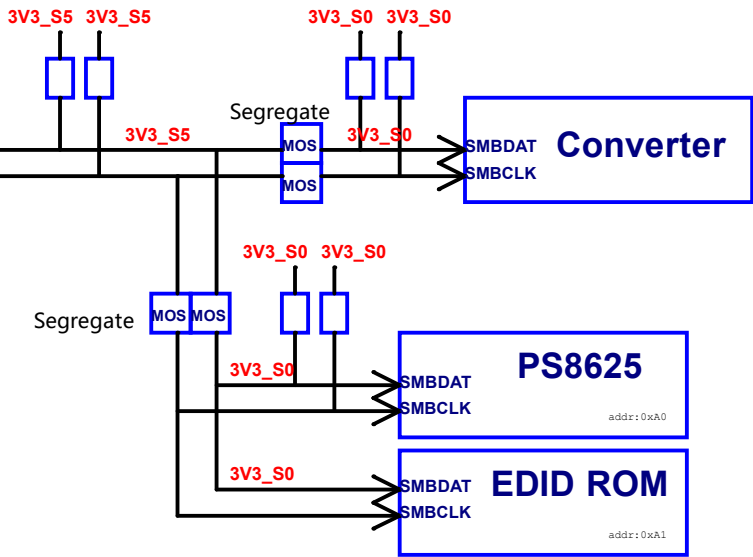
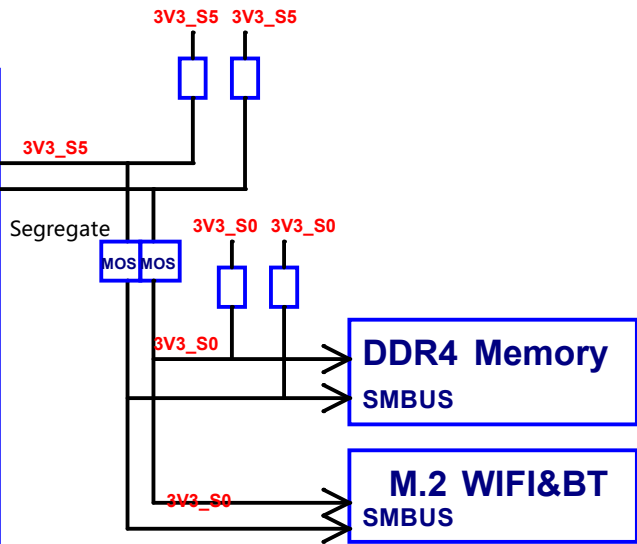
Fig 12. Gate-source threshold voltage as a function of junction temperature

BITLAND		Bitland Information Technology Co., Ltd.	
Title: Hole/BOSS/MOS Spec			
Size	Document	Number	Rev
Custom	IGMLSB		1.0
Date:	Tuesday, February 27, 2018	Sheet	39 of 47

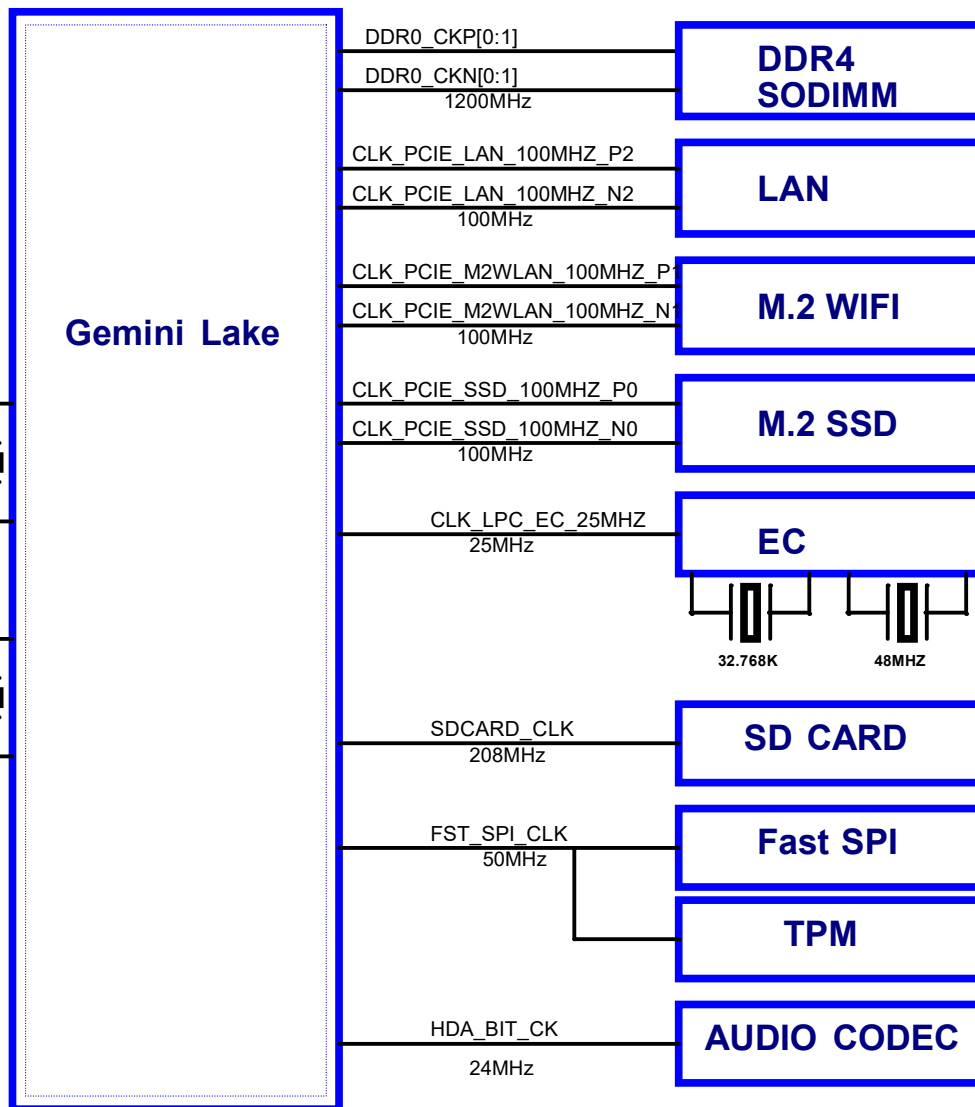


# Power Delivery Diagram

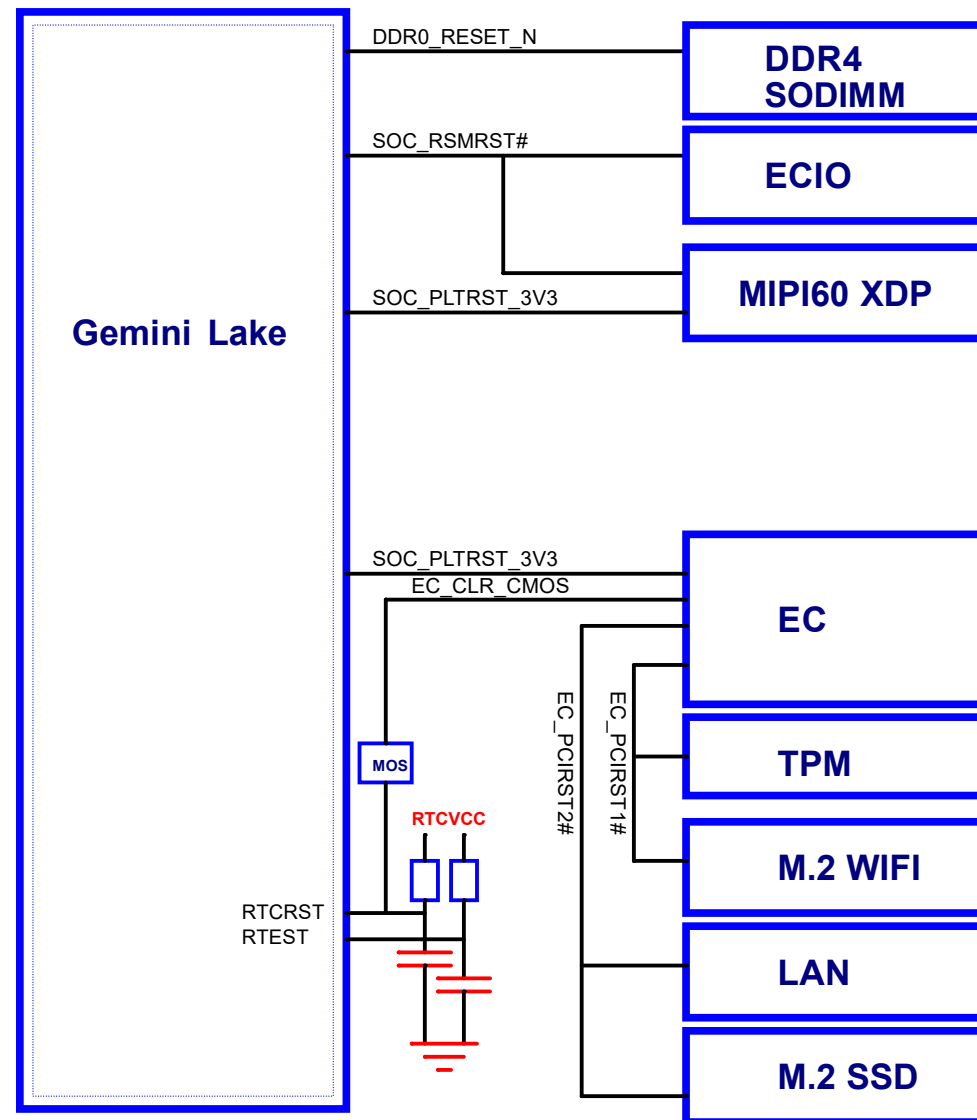




## CLOCK MAP



## RESET MAP



Level Shift Table

Item	Source	Signal Name	Destination	Signal Name	Remark
1	USB3.0_1	UART_USB_SEL	SOC	SOC_GP29_R	3V3_S5--LSI1012LT1G--1V8_S5
2	ECIO	EC_SCI#	SOC	SOC_GPIO_38	3V3_S5--LSI1012LT1G--1V8_S5
3	ECIO	EC_DIS_TURBO	SOC	SOC_GP23	3V3_S5--LSI1012LT1G--1V8_S5
4	ECIO	EC_PL1_ADJ	SOC	SOC_GP24	3V3_S5--LSI1012LT1G--1V8_S5
5	ECIO	KRST#	SOC	SOC_GP26	3V3_S0--BSS138/BSS138--1V8_S5
6	ECIO	EC_SMI#	SOC	SOC_GPIO_41	3V3_S5--LSI1012LT1G--1V8_S5
7	ECIO	EC_PROCHOT#	SOC	PROCHOT_N	3V3_S5--LSI1012LT1G--1V8_S5
8	SOC	THERMALTRIP_R	ECIO	THERMALTRIP_N_EC	1V8_S5--LSI1012LT1G--3V3_S5

USB OC Setting

Function	OC port	USB port	Device
USB3.0_OC	USB_OC_1	USB3.0_1&USB3.0_2	USB3.0 CONN
USB2.0_OC	USB_OC_0	USB2.0_1~USB2.0_4	USB2.0 CONN

SoC-GPIO function

Pin Name	Power Well	Usage	Boot Set
SOC_GPIO_41	+1V8_S5	EC_SMI#	GPI
SOC_GPIO_38	+1V8_S5	EC_SCI#	GPI
SOC_GPIO_34	+1V8_S5	SW_CLR_CMOS	GPI
SOC_GPIO_19	+1V8_S5	LPCPD#	GPO
SIO_UART2_CTS#	+1V8_S5	TPM_SPI_IRQ_L	GPI
SOC_GPIO_30	+1V8_S5	SOC_TPM_Mark	GPI
SOC_GPIO_29	+1V8_S5	UART_USB_SEL	GPI
SOC_GPIO_26	+1V8_S5	KRST#	GPI
SOC_GPIO_23	+1V8_S5	EC_DIS_TURBO	GPI
SOC_GPIO_24	+1V8_S5	EC_PL1_ADJ	GPI

EC-GPIO Function

ECIO IT8738E/EX GPIO Table								
GPIO Name	P/N	Set	Type	Voltage	Default	Pull High/Low RES	Function	Remark
GP13	30	GPO	DIOD8	+3V3_S0	GPO	R658(Dummy)/None	LPC_CLKRUN_N	LPC_CLKRUN_N
GP14	29	GPI	DIOD8	3.3VSB	GPO	R588/None	PID2	Panel ID 2
GP17	26	GPI	DIOD8	3.3VSB	GPI	R590/None	PID0	Panel ID 0
GP20	25	GPI	DIOD8	3.3VSB	GPI	R589/None	PID1	Panel ID 1
GP21	24	GPO	DIOD8	3.3VSB	GPI	R507/None	HW_POP_MUTE_EC_L	High=Don't Mute,Low=Mute
GP24	21	GPO	DIOD8	3.3VSB	GPI	R498/None	EC_PL1_ADJ	BIOS 內 需增加ASL code 來做這兩pin 變動時更改 platform 設定 Ex
GP25	20	GPO	DIOD8	3.3VSB	GPI	R310/None	BT_DISABLE	M.2 Bluetooth on/off,H:Enable,L:Disable
GP26	19	GPO	DIOD8	3.3VSB	GPI	R305/None	WLAN_DISABLE	M.2 WIFI on/off,H:Enable,L:Disable
GP27	18	GPO	DIOD8	3.3VSB	GPI	RA1/None	BEEP_EC	BEEP output from EC
GP31	16	GPO	DIOD8	3.3VSB	GPO	R497/None	EC_DIS_TURBO	BIOS 內 需增加ASL code 來做這兩pin 變動時更改 platform 設定 Ex
GP32	15	GPI	DIOD8	3.3VSB	GPO	R586/None	EC_BL_EN_DET	Backlight enable detect ,H:Enable,L:Disable
GP36	14	GPO	DIOD8	3.3VDSW	GPO	R385/None	EC_PWR_LED	Power LED:S0/S1 on,S3 Blinking,S4/S5 off
GP37	12	GPO	DIOD8	3.3VSB	GPI	R45/None	EC_SMI#	SMI#
GP52	10	GPO	DIOD8	3.3VSB	GPI	R506/None	EC_SCI#	SCI#
GP70	102	GPI	DIOD8	3.3VSB	GPI	R109/None	EC_PROCHOT#	EC_PROCHOT#,ACTIVE LOW
GP72	104	GPO	DIOD8	3.3VSB	GPI	PR77/None	1V05_PG_TO_EC	1V05_PG_TO_EC
GP74	106	GPI	DIOD8	3.3VSB	GPI	R123(Dummy)/None	SUSPWRDNACK_EC	SUSPWRDNACK
GP75	107	GPO	DIOD8	3.3VSB	GPI	R118/None	EC_CLR_CMOS	POWER BITTON CLEAR CMOS
GP80	94	GPI	DIOD8	3.3VSB	GPI	R431/R434	ECIO_GP80(Board ID0)	Reserve 3 GPIO(3.3VSB) For different SKU
GP81	95	GPI	DIOD8	3.3VSB	GPI	R430/R433	ECIO_GP81(Board ID1)	Reserve 3 GPIO(3.3VSB) For different SKU
GP82	96	GPI	DIOD8	3.3VSB	GPI	R429/R432	ECIO_GP82(Board ID2)	Reserve 3 GPIO(3.3VSB) For different SKU
GP83	97	GPO	DIOD8	3.3VSB	GPI	R500/None	EC_OVERRIDE	EC_OVERRIDE
GP84	98	GPI	DIOD8	3.3VSB	GPI	R418/R422	SOC_TPM_ID0	ID for TPM
GP87	99	GPI	DIOD8	3.3VSB	GPI	R419/R423	SOC_TPM_ID1	ID for TPM
GPB0	122	GPI	DIOD8	3.3VSB	GPO	PR34/None	5V_3V3_S5_PWRGD_R	5V_3V3_S5_PWRGD
GPB1	123	GPI	DIOD8	3.3VSB	GPI	R504(Dummy)/None	UARTA_P80_EN	UARTA 80 port enable
GP71	103	GPI	DIOD8	3.3VSB	GPI	R119/None	THERMALTRIP_N_EC	THERMALTRIP
GPB6	128	GPI	DIOD8	3.3VDSW	GPI	R518/None	COM1_RI_L	LAN WAKE UP(G3 To S5)
GPB4	126	GPO	DIOD8	3.3VSB	GPO	R247/None	EC_GPB4	High=Nomal,Low=Enable online update
GPB5	127	GPO	DIOD8	3.3VSB	GPI	R259/None	EC_GPB5	High=Nomal,Low=Enable online update
GP76	105	GPI	DIOD8	3.3VSB	GPI	R635/None	SLP_S3_N_3P3_DEY	Delay from SLP_S3_EC_N_3P3 to control 1V05_S5S0 Power
GPB0	122	GPI	DIOD8	3.3VSB	GPO	R127(Dummy)/None	SLP_S0_EC_N_3P3	SLP_S0ix
GP72	104	GPO	DIOD8	3.3VSB	GPI	R644/None	VTT_CNTL_SOIX	Delay from SLP_S0_EC_N_3P3 to control S0ix Power



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Title

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Table 2-28. Hardware Straps (Sheet 1 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable <b>Note:</b> If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override <b>Note:</b> This strap enables the platform to override security features in the SPI.
GPIO_43	MDSI_C_TE	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	USB2_OC0_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) <b>Note:</b> Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) <b>Note:</b> This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.
GPIO_62	SIO_UART0_RTS_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

Table 2-28. Hardware Straps (Sheet 2 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) <b>Notes:</b> 1. DnX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would download a new firmware image from a recovery host, over USB, and overwrite the image in the storage media. TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) <b>Note:</b> The board should strap this low and do not use otherwise
GPIO_79	SIO_SPI_0_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_80	SIO_SPI_0_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_81	SIO_SPI_0_FS1	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_85	SIO_SPI_2_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

GPIO_87	SIO_SPI_2_FS2	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_89	SIO_SPI_2_TXD	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_159	AVS_I2S0_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_163	AVS_I2S1_WS_SY NC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) <b>Note:</b> Platforms should strap this LOW. Functionality is handled by the PMC.
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)

Table 2-28. Hardware Straps (Sheet 3 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.
GPIO_177	SMB_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_191	CNV_BRI_DT	eSPI Flash Sharing Mode	20K PD	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS; default) Note: if eSPI mode is disabled (eSPI/LPC hard strap(GPIO_175) is set to select LPC) then the eSPI slave attached flash sharing strap must also be set to 0.
GPIO_192	CNV_BRI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_193	CNV_RGI_DT	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_194	CNV_RGI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_195	CNV_RF_RESET_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_196	XTAL_CLKREQ	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

REVISION HISTORY:

Rev	Date	Notes
0.1	20170505	First release
Rev	Date	Notes
0.2	20170712	<div>1.Page05, Delete HPD Pull down Res R670 to follow PDG 1.2 page 269;</div> <div>2.Page07, Board I/O GPIO configuration table;</div> <div>3.Page09, add C905,C907,C908,C909 to fix LPC/FSPI SI issue, R83 change to 33 ohm</div> <div>4.Page10, Y2 RTC 32.768K Change to use 5PPM XTAL,C13&amp;C15 change to 3.3PF for SI issue, R105 change to 20 K_F, Delete C23</div> <div>5.Page12, Delete R685 stuff C903 Short VNNAONT to VDD2_AUDI SHF or Layout easy</div> <div>6.Page15, C145 Change to 0.1u for ESD issue;</div> <div>7.Page16, Swap Q16&amp;Q18 Do Sfring up issue Delete BKLCTL Level shift reversed circuit.</div> <div>8.Page17, Delete BKLTEN Level shift reversed circuit;</div> <div>9.Page18, Dummy R646,stuff R647,R647 pull high change to +1V8_S5;Dummy L2/L3/L4/L5, stuff R282 R283 284 285 R287 R288 R289 R290 to fix HDMI S issue BM pass</div> <div>10.Page20, Change the SSD Boss footprint;</div> <div>11.Page22, Stuff R686 to enable SD_CLKREQ function,R679 Change to 2.2 ohm,C895 Change to 3.3pf for EMI</div> <div>12.Page23, USB2.0_1,USB2.0_4,USB3.0_2 use common load switch and cap;</div> <div>13.Page24, USB3.0_1,USB2.0_3,USB2.0_2 use common load switch and cap;</div> <div>14.Page26, Change TPM to NPCT652LBAYX(Nuvoton)(Main) &amp; SLB 9670VQ2.0(Infineon)(sub);</div> <div>15.Page27, PCIRST1 is used as VTT_CNTL_S0IX, PC RST2 to enable SD_WR/ LAM SSD TPMP C RST3 is used as SLP_S3_N_3P3_DEY</div> <div>16.Page27, Stuff R428&amp;R424,Dummy R425;</div> <div>17.Page33, Stuff PR247 &amp; PR245,add SLP_S3_EC_N_3P3 &amp; SLP_S0_EC_N_3P3 to enable +1V05_S5S0,PR82 change to 10K,PC104 change to 0.1uf to fix SI issue;</div> <div>18.Page36, PC189 change to Q0402 foot print, stuff PR147, PR153 PR155 PR157, PR158 for SV D VNN</div> <div>19.Page38, add standby power discharge circuit,add C913,C914,C915,C916,C917,C918 for ESD issue.</div> <div>Power modify list:</div> <div>1.PR97 change to 10.5K form 10.2K for 1.2V</div> <div>2.PR176 change to 1K VNN OCP :11.12A</div> <div>3.PR128 change to 1.87K ; PR120 change to 30K 温度: PQ13: 108° PQ14: 82° R6: 7</div> <div>4.PR137 change to 1 OHM PC153 change to 3300Pf for VCCGI High MOS VDS</div> <div>5.PQ13+PQ14/PQ15 change to PK616BA+PK618BA</div> <div>6.PR86 change to 10.2K.</div> <div>7.VCCGI VTT TEST</div> <div>PC157 remove</div> <div>PC159 change to 0.22UF</div> <div>PR145 change to 390</div> <div>PR131 change to 3.47K</div> <div>PC162 change to 4700PF</div> <div>PR146 change to 1K</div> <div>PC134 change to 8200PF</div> <div>PR130 change to 3K</div> <div>PC139 change to 820PF</div> <div>8.VNN choke change to 0.47uH</div> <div>1004-02120Power Inductor 0.47uH ± 20 %4 2 mΩ 17. 5A 26A7.2*6.6* 3 mm TIO BM 47 BM05V09-L1 SM HF</div> <div>Choke PL7 0.47uh,</div> <div>PC166 change to 10NF</div> <div>PC167 change to 56PF</div> <div>PR162 change to 4.02K</div> <div>PC171 AND PR164 REMOVE</div> <div>PR177 change to 1K</div> <div>PC192 change to 2200PF</div> <div>9.IC stress test</div> <div>VCCGI Vout 390uF cap change to 220uF. 4PCS 47uF MLCC delete.</div>

REVISION HISTORY:

Rev	Date	Notes
0.3	20170911	1.Page09,C905,C907,C908 change to 39pf for SI issue; 2.Page10,add C919 & C920 for SI issue 3.Page14,R213& R214 change to 10 ohm,C150&C151 Change to 22 PF for SI issue.R207 change to 240 ohm to follow Intel MOW WW32; 4.Page26,Dummy R417,stuff R411, change the TP Mstrapping SIT dot have T PMf und i o; 5.Page28,RTL8111H-CG change to RTL8111G-CG for LAN Surge issue; 6.Page29,R562 change to 1.87K,dummy CA2 & CA3 for no beep issue, Dummy C416 for SI issue;R537,R538,R539,R540 change to 30 ohm bead for SI & EMI test; 7.Page38,R579 &R575 change to 169 ohm to follow INTEL MOW; 8.Page34,PL5>1.5UH/PR92->1ohm/PC115->1000PF for thermal test 9.Page07,QT/YT/AIO330 SKU configuration GPIO. Power change list: 1.PC21 改 47uF FOR VSYS1 NRSHU 2.VCCGI second source 漏孔 Hide 改 S M508 1007- 01 B 3.PR122 93.1k change to 82.5K. lmon 漏 4.PC157 stuff 0.022UF/25V,X7R 5.PC140 chagne 330pF/1001-00398 6.PR251 change to 0 ohm 7.PR92/PC115 change to 1ohm+1000pF for PEC6/PL5 thermal. 8. PR181,PR183,PR184,PR186 change to r0402_short pad.

Rev	Date	Notes
0.4	20180102	1.Page18,R293,R294,R295,R296 change to 4.7K for DDC SI; 2.Page14,Delete R187 for ME issue; 3.Page06,ADD D43 AZ124S-04F for Down USB 3.0 to fix ESD issue; 4.Page15,SODIMM slot change to 1011-07427 (ADDR0205 P023A1)

Rev	Date	Notes
1.0	20180227	update to V1.0